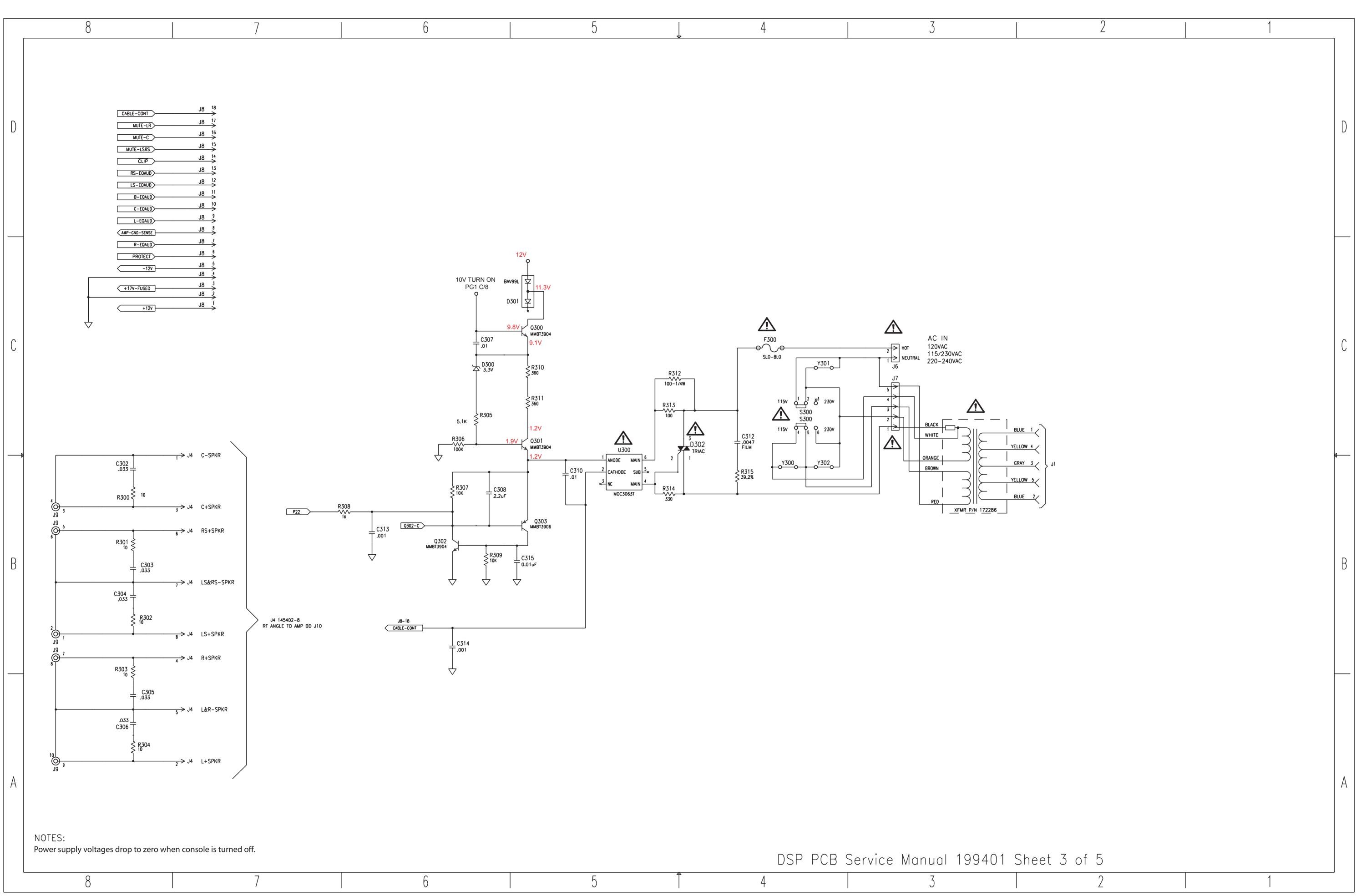
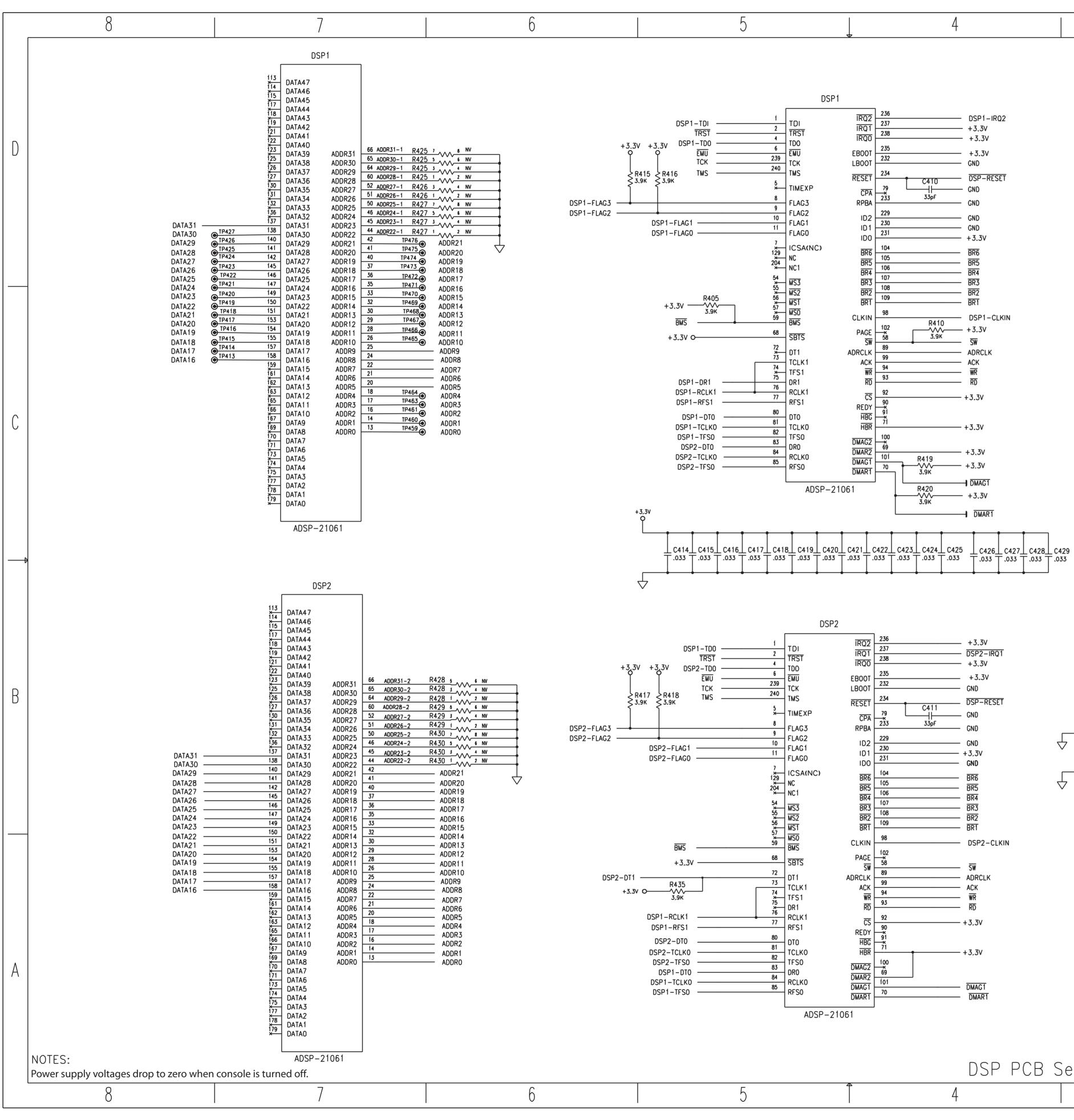


5	1 4	3	



5 4 3 1		<u>د</u>	4	_
	3	4		5



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C402

33pF

C403

33pF

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R412

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DSP1-CLKIN

DSP2-CLKIN

JTAG-CLKIN

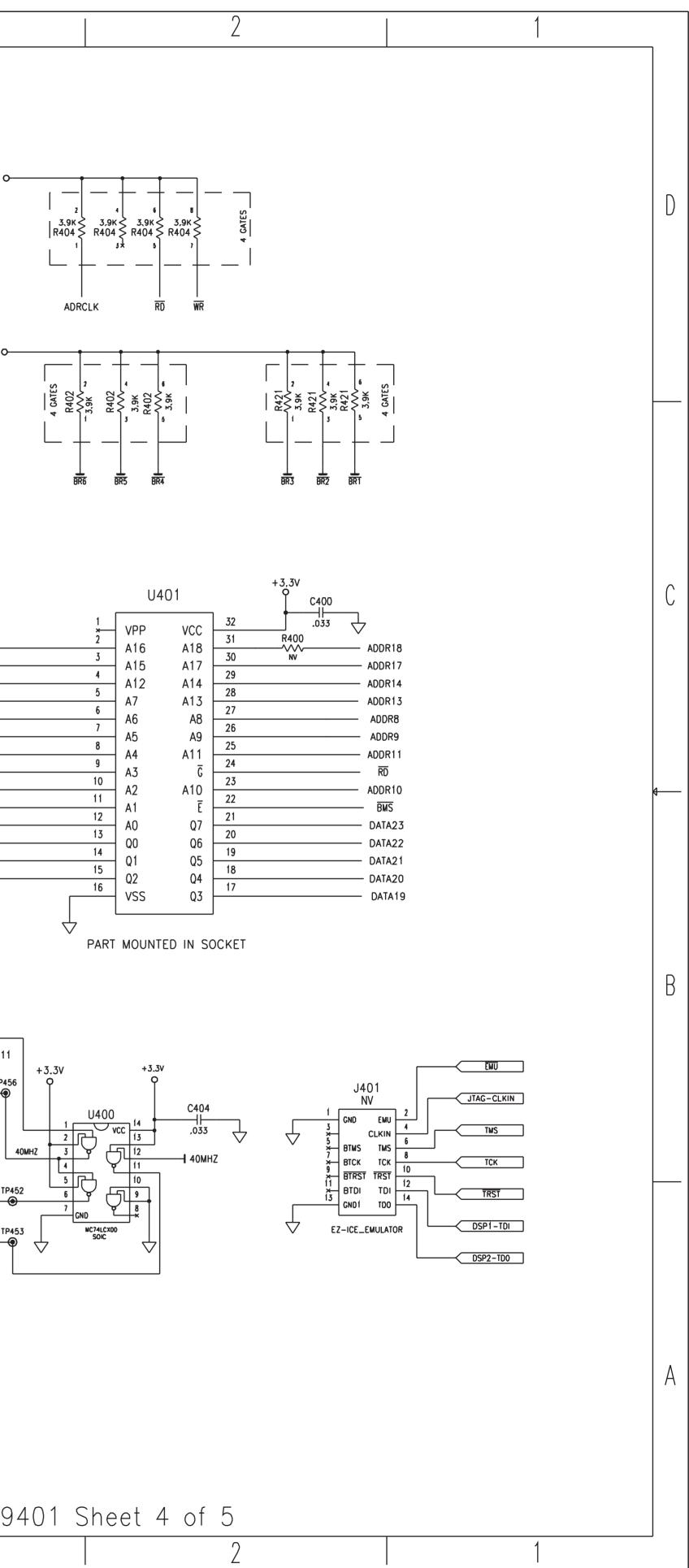
CR400 40MHz HC-49/S

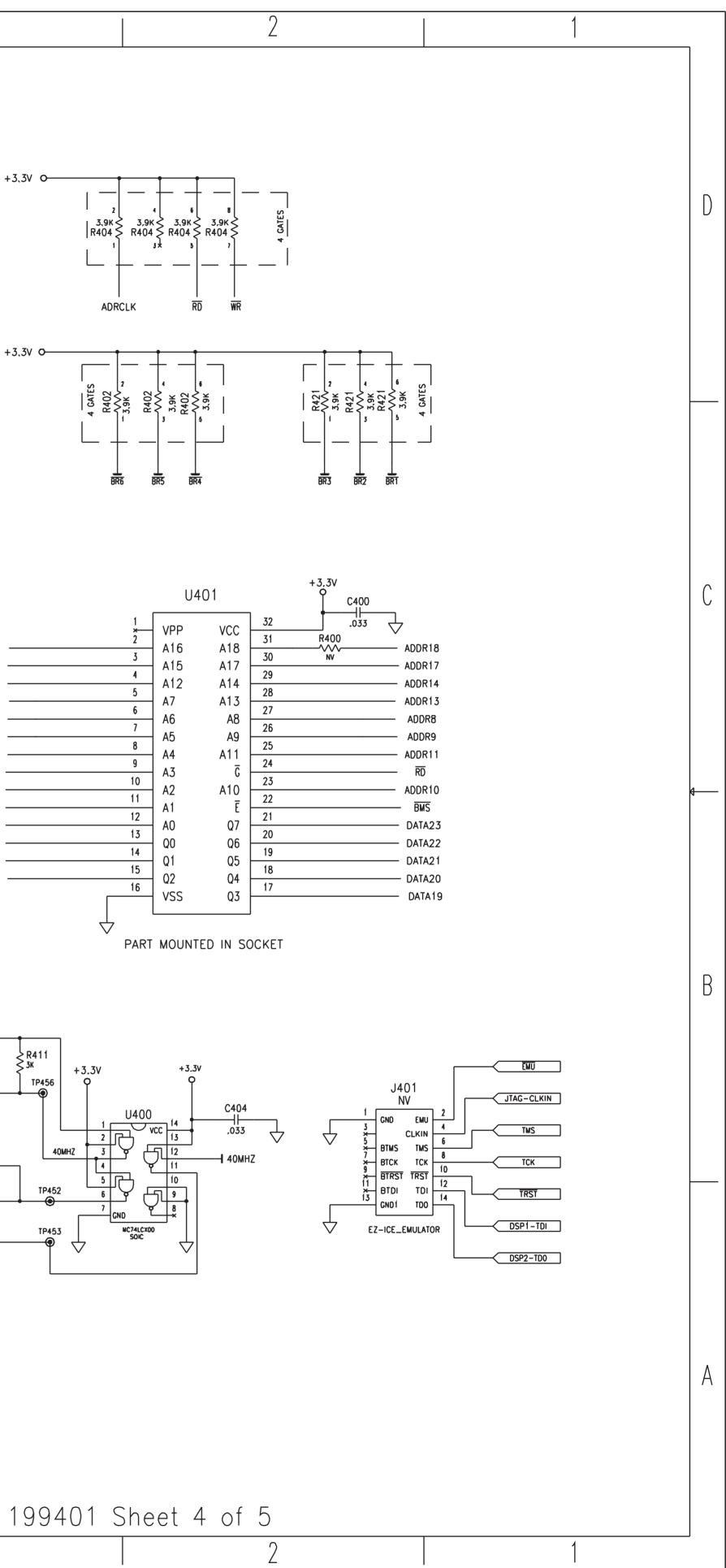
R409

R407

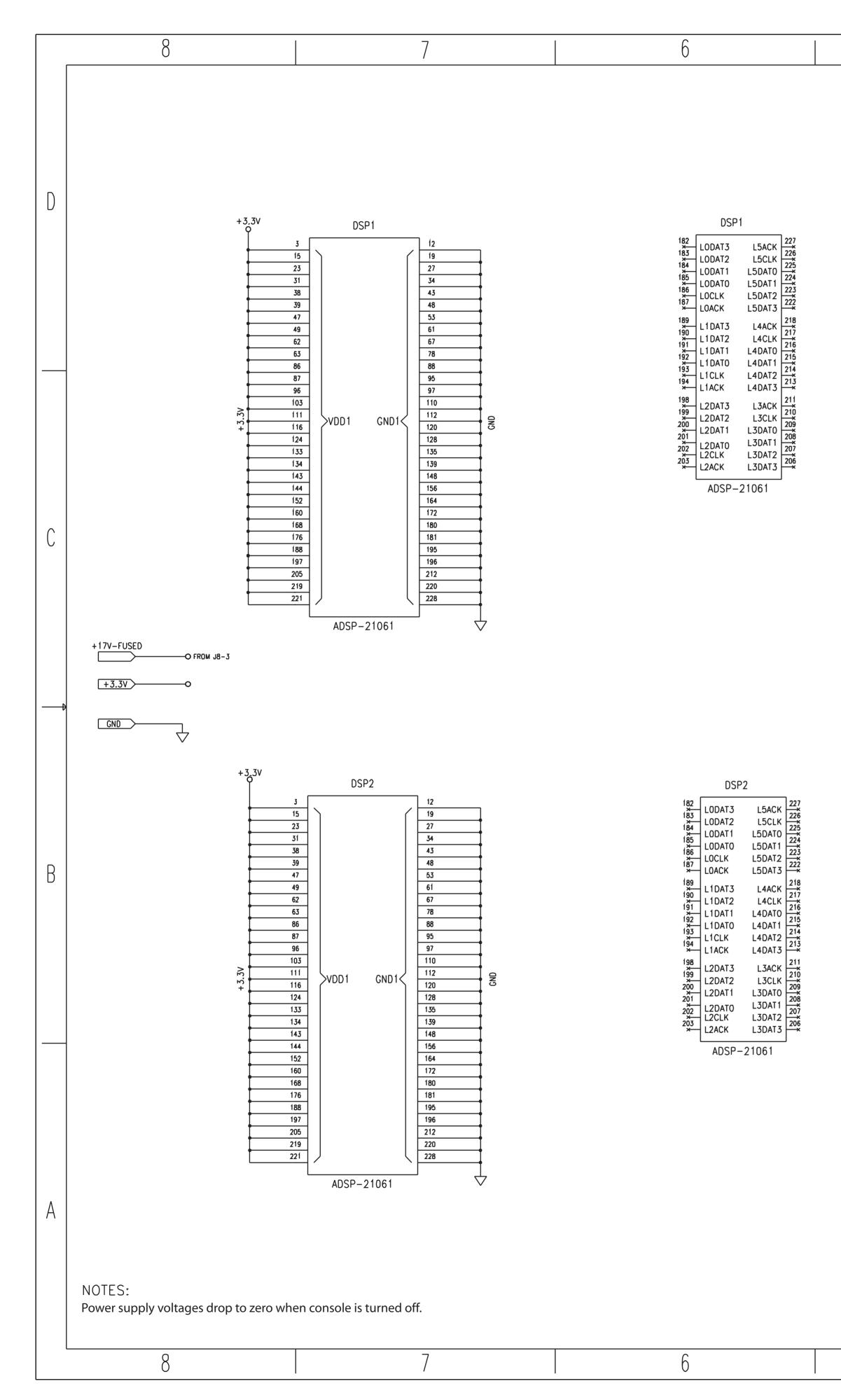
5 1 4 3		00		Sheet
	5	4	3	

		1 ×	VPP
ADDR16		2	A16
ADDR15		3	A15
		4	
ADDR12		5	A12
ADDR7		6	A7
ADDR6		7	A6
ADDR5		8	A5
ADDR4			A4
ADDR3		9	A3
ADDR2		10	A2
ADDR1		11	A1
ADDR0		12	AO
DATA16		13	QO
DATA17		14	
		15	Q1
DATA18		16	Q2
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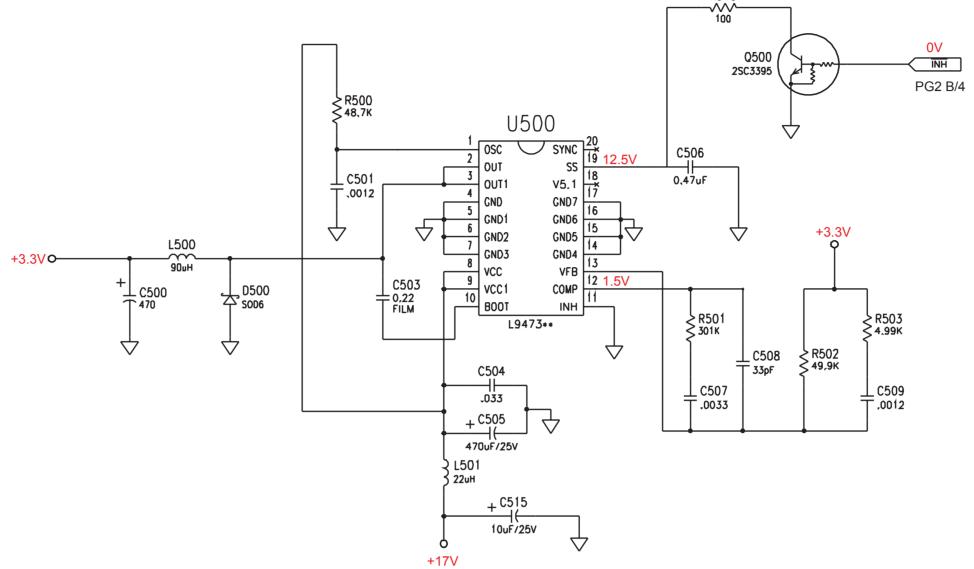




5	4	3	



5	4	3	



5		4		3		2		
	R500 48,7K	U500 1 OSC SYNC 2 OUT SS 0 UT V5.1 4 CND CND7 5 CND1 GND6 15	R510 100 25C3395 C506 0,47uF		for approximately 5 secor	V will be present at the base of Q50 nds to allow pin 19 of U500 to be p lator. The 3.3V supply is turned off a down sequence.	ulled	D
		0 GND2 GND5 13 7 GND3 GND4 13	R501 301κ	+3.3V R503 4.99K C509 .0012				С
								B
5		DSP PCE	3 Service M	anual 19940 3	1 Sheet 5 o	of 5		A