EK9716

Rev. 0.4

PRELIMINARY DATA SHEET

1200CH TFT LCD
Source Driver with TCON

fitipower integrated technology Inc.

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1200CH TFT LCD Source Driver with TCON

1. GENERAL DESCRIPTION

EK9716 is a highly integrated 1200 channel source driver with TTL interface Timing Controller for color TFT-LCD panels. EK9716 integrated source driver, timing controller and pin control interface.

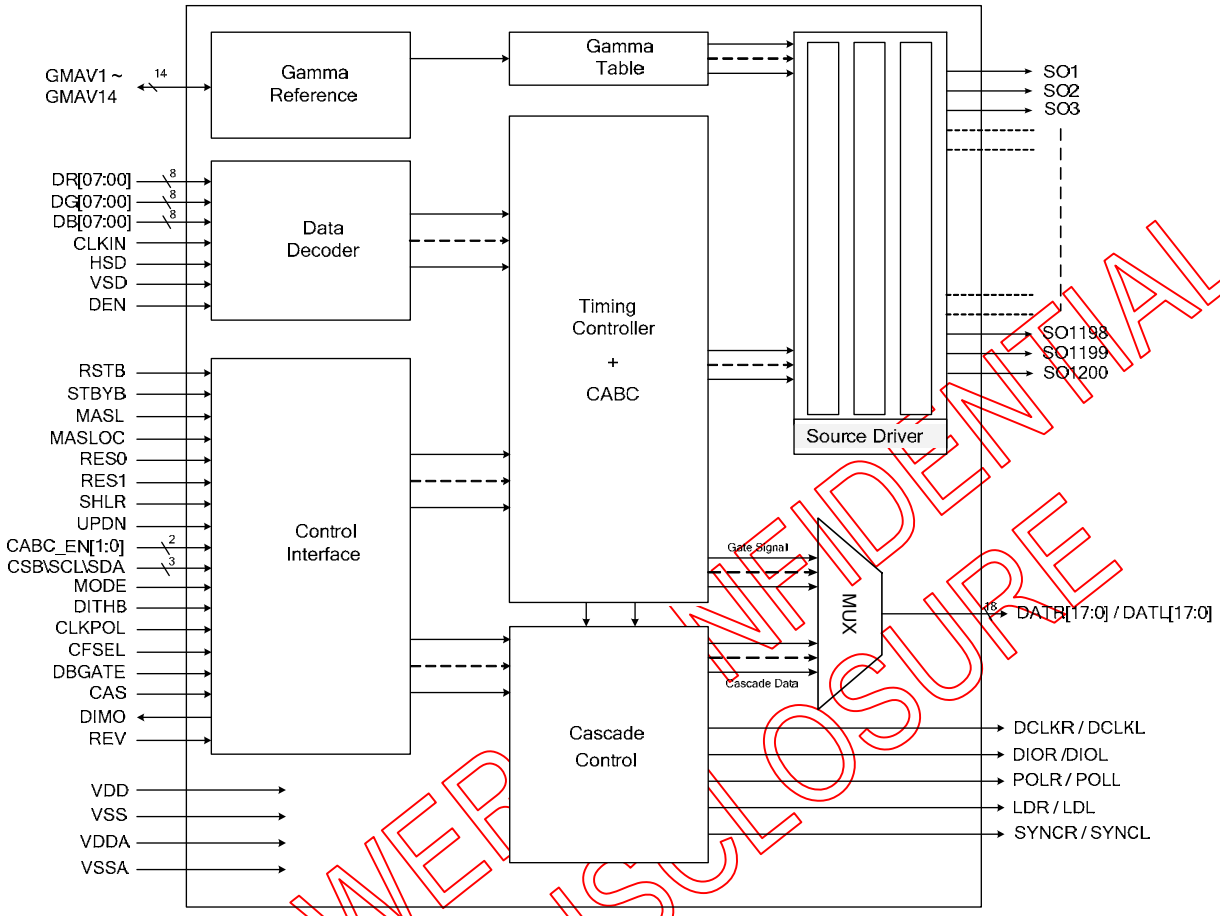
EK9716 input timing support TTL digital 24bit parallel RGB data format, and source output support 8-bit resolution 256 gray scales with dithering features. Operating parameters can be set via pin control for all control features. Special circuit architecture is designed for lower power dissipation.

EK9716 support two chip cascade operation mode to reduce the FPC amount and save the cost. Configure able Master and Slave configuration increase the flexibility for different panel design. With wide range of supply voltages and small output deviations make this chip more suitable for various applications.

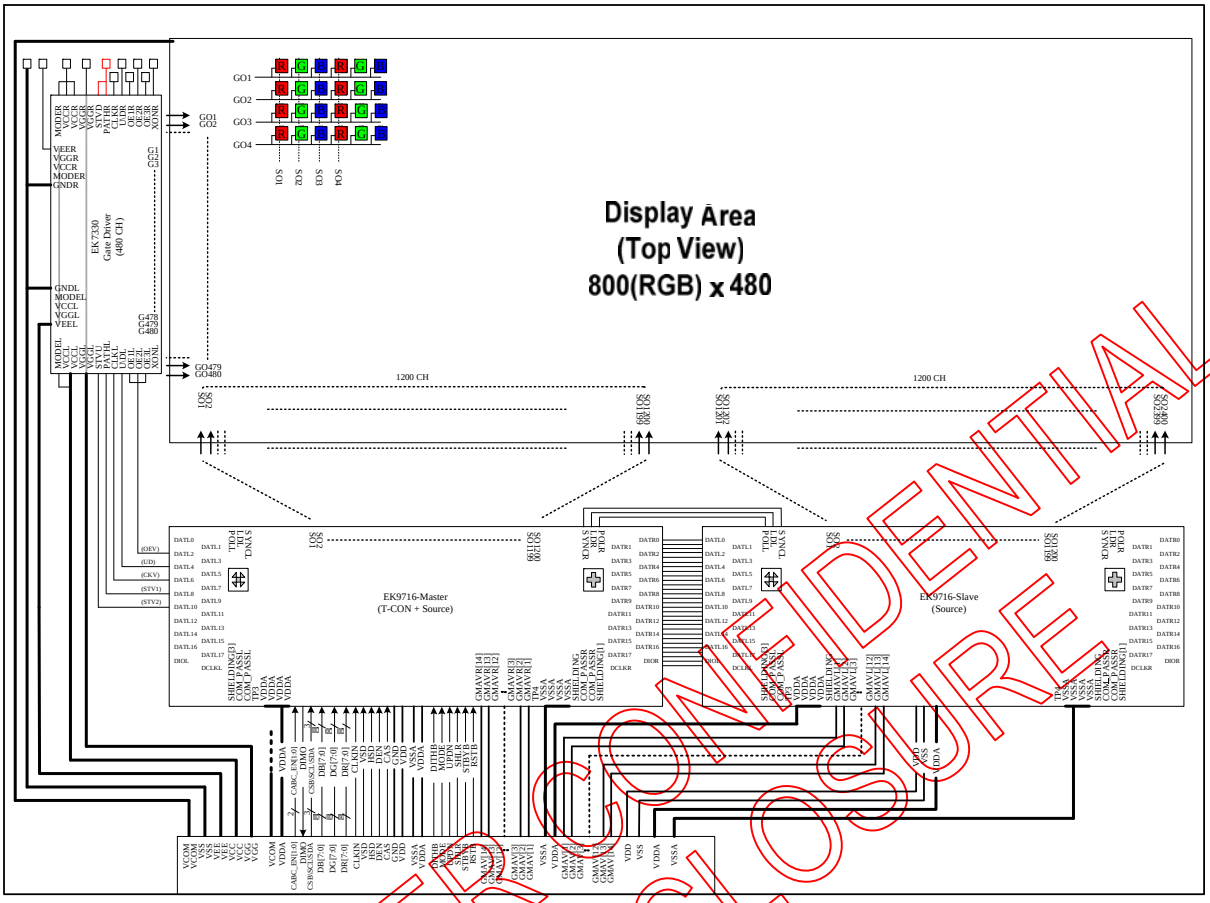
2. FEATURES

Special design for small-sized color TFT LCD source drivers with timing controller
Integrated 1200 channel source driver
Support display resolutions : 800(RGB)x600、800(RGB)x480、400(RGB)x480、400(RGB)x240
8-bit resolution 256 gray scale with 2-bits dithering (6bits DAC + 2bits HFRC)
Support TTL 24-bit parallel (RGB) input timing
Support cascade function with bidirectional shift control (CMOS signal)
Support single or dual-gate operation mode
Support Delta or Stripe color filter configuration
Support stand-by mode for low power consumption
Support dot inversion driving scheme (Cascade mode)
Support 2 dot one inversion driving scheme (Dual Gate mode)
V1 ~ V14 for adjusting Gamma correction
Output dynamic range: 0.1V ~ VDDA-0.1V (Dual Gate mode)
Power for source driver voltage VDDA: 6.5V ~ 13.5V
Power for digital interface circuit VDD: 2.7 ~ 3.6V
Max. operating frequency: 50 MHz
Minimum operating frequency: 20 MHz (800(RGB)x600 and 800(RGB)x480 display resolution)
Built-in CABC function
Built-in AUTO pattern
COG package
Chip Size: 22572um X 938um, Output Pad Pitch: 17um

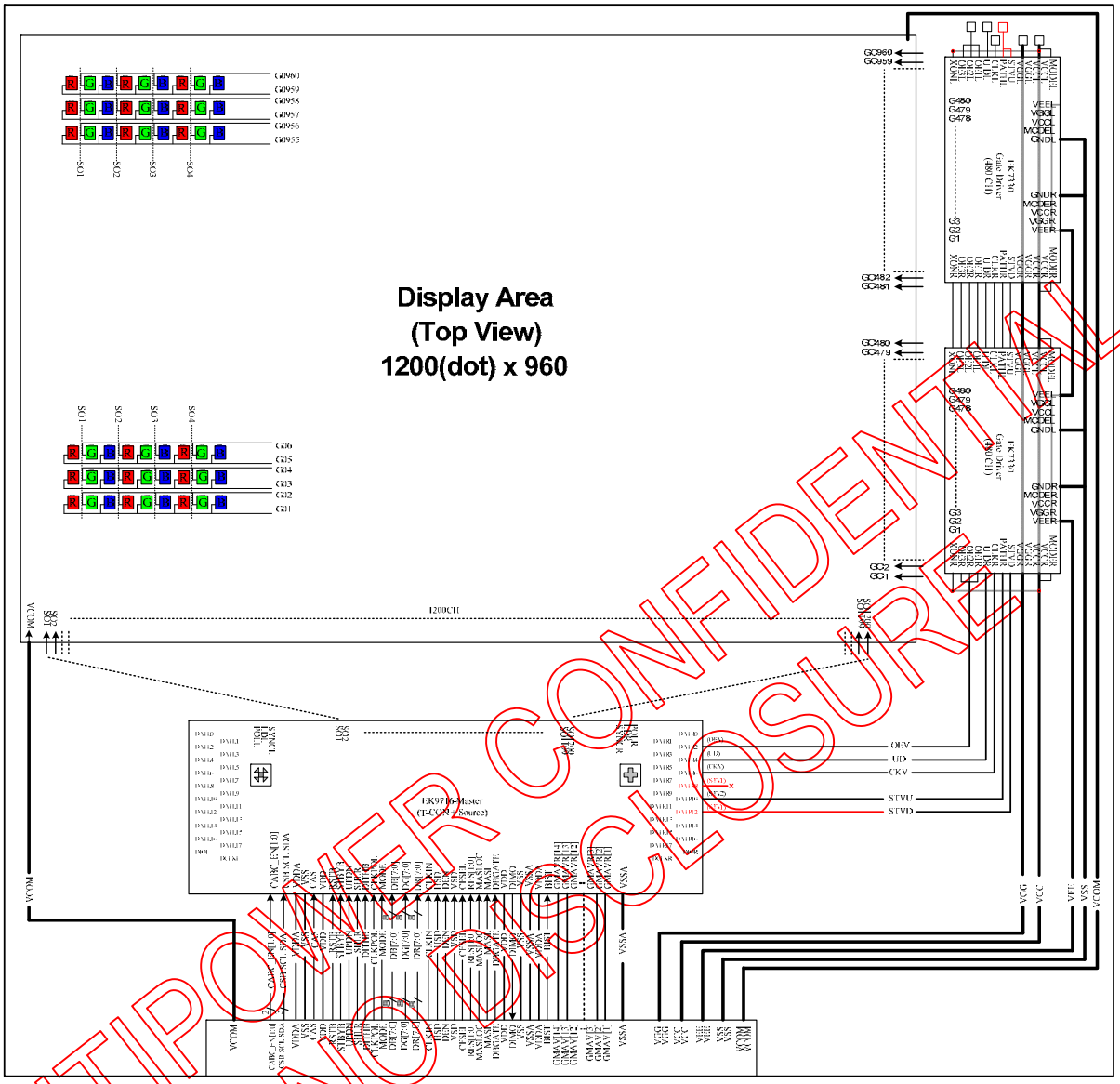
3. BLOCK DIAGRAM



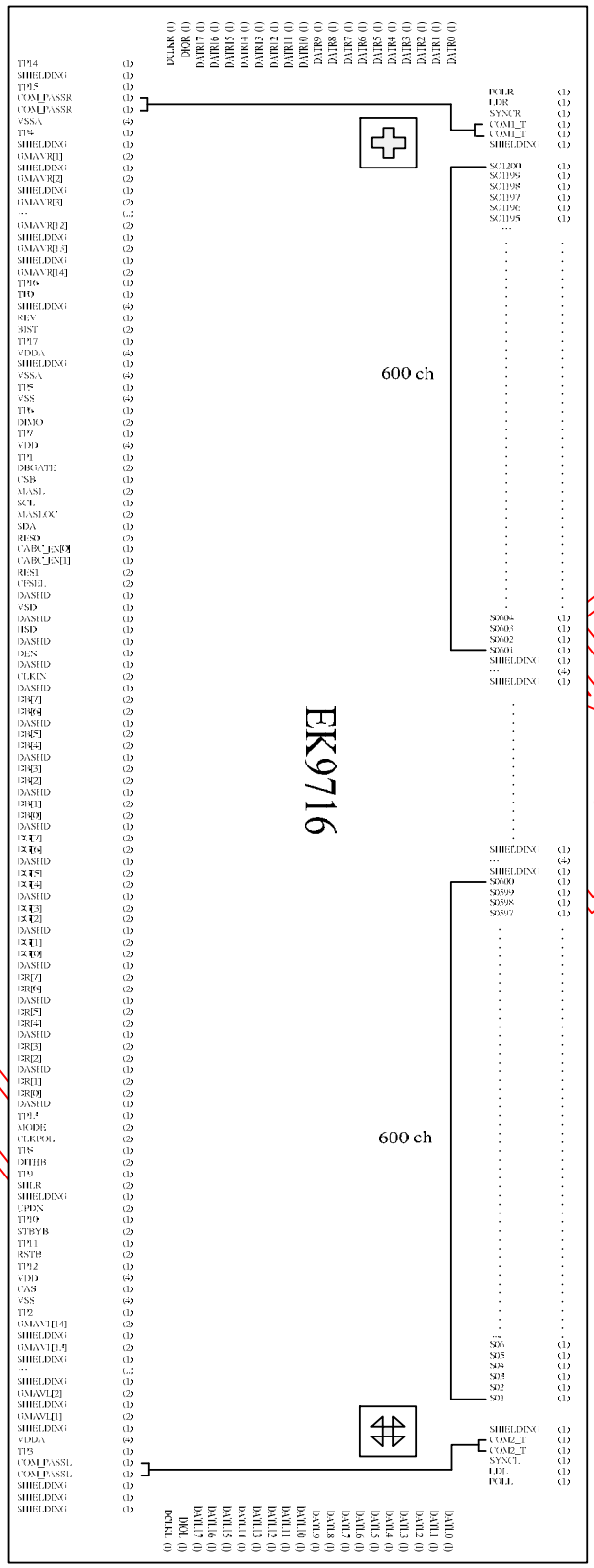
Block Diagram

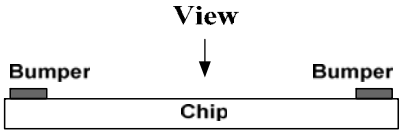


Application Block Diagram — 2 Chip Cascade



Application Block Diagram – Dual Gate Application





Pad Sequence (Bump Side)

4. PIN DESCRIPTION

Pin Description

Pin Name	Pin Type	Description
DR[07:00] DG[07:00] DB[07:00]	Input	Parallel data Input. For TTL 24-bit parallel RGB image data input. DR[07:00]=R[7:0] data; DG[07:00]=G[7:0] data; DB[07:00]=B[7:0] data. For 18bit RGB interface, connect two LSB bits of all the R/G/B data buses to VSS.
CLKIN	Input	Clock for Input Data. Data latched at rising/falling edge of this signal. Default falling edge.
HSD	Input	Horizontal Sync input. Negative polarity.
VSD	Input	Vertical Sync input. Negative polarity.
DEN	Input	Data Input Enable. Active High to enable the data input bus under "DE Mode". Normally pull low.
MODE	Input	DE / SYNC mode select. Normally pull high H: DE mode.(Default) L: HSD/VSD mode.
RES[1:0]	Input	Display resolution selection. RES[1:0] = "00", for 800(RGB)*480 display resolution(Default) RES[1:0] = "01", for 800(RGB)*600 display resolution RES[1:0] = "10", for 400(RGB)*480 display resolution RES[1:0] = "11", for 400(RGB)*240 display resolution
DITHB	Input	Dithering function enable control. Normally pull high DITHB = "1", Disable internal dithering function(Default) DITHB = "0", Enable internal dithering function
CLKPOL	Input	Input clock edge selection. Normally pull low CLKPOL = "1", Latch data at CLKIN rising edge. CLKPOL = "0", Latch data at CLKIN falling edge. (Default)
DIMO	Output	Backlight dimmer signal for CABC application DIMO = "0", Turn off external backlight controller DIMO = "1", Logical control signal to turn on external backlight controller Note: Refer to the Power On/Off Sequence for the detail information
CABC_EN[1:0]	Input	CABC H/W enable pin. Normally pull low When CABC_EN = "00", CABC OFF.(Default mode) When CABC_EN = "01", User interface Image When CABC_EN = "10", Still Picture When CABC_EN = "11", Moving Image
CFSEL	Input	Color Filter type selection. Normally pull high CFSEL = "1", Stripe mode. (Default) CFSEL = "0", Delta mode
DBGATE	Input	Dual Gate function enables control. Normally pull low DBGATE = "1", Enable Dual Gate Function. DBGATE = "0", Disable Dual Gate Function (Default) Note: Cascade function will be disabled under "dual gate" mode
GMAV1 ~ GMAV14	Input/Output	Gamma correction reference voltage. These input voltage must be offered by user. VSSA+0.1<V14<V12<V11<V10<V8;V7<V5<V4<V3<V1< VDDA-0.1 (Dual Gate) VSSA+1<V14<V12<V11<V10<V8;V7<V5<V4<V3<V1< VDDA-1 (Cascade mode) V2, V6, V9, V13 pads are disabled.
RSTB	Input	Global reset pin. Active Low to enter Reset State. Suggest to connecting with an RC reset circuit for stability. Normally pull high.

Pin Name	Pin Type	Description
STBYB	Input	Standby mode, Normally pull high. STBYB = “1”, normal operation(Default) STBYB = “0”, timing controller, source driver will turn off, all output are High-Z
MASL	Input	Master and Slave Mode selection. Normally pull high. MASL = ”H”, for Master mode. (Default Mode) MASL = ”L”, for Slave mode. Only the Master chip will issue the Gate and Cascade control signal.
MASLOC	Input	Master location definition pin. Normally pull low. MASLOC = ”L”, Master locate on right side (Panel top view). (Default Mode) MASLOC = ”H”, Master locate on left side (Panel top view).
CSB	Input	Serial communication chip select. Normally pull high
SDA	Input/Output	Serial communication data input. Normally pull low
SCL	Input	Serial communication clock input. Normally pull low
SHLR	Input	Source Right or Left sequence control. Normally pull high. SHLR = “L”, shift left: last data = S1←S2←S3……←S1200 = first data. SHLR = “H”, shift right: first data = S1→S2→S3……→S1200 = last data.
UPDN	Input	Gate Up or Down scan control. Normally pull low. UPDN = “L”, STV2 output vertical start pulse and UD pin output logical “0” to Gate driver.(Default) UPDN = “H”, STV1 output vertical start pulse and UD pin output logical “1” to Gate driver.
BIST	Input	Normal Operation/BIST pattern select. Normally pull low BIST = H : BIST(DCLK input is not needed) BIST = L : Normal Operation
CAS	Input	Cascade function select. Normally pull high. CAS = ”H”, Enable cascade function.(Default) CAS = ”L”, Disable cascade function.
REV	Input	Controls whether the data of D00~D27 are inverted or not, normally pulled low. When “REV”=1 these data will be inverted. EX. “00” → “ 3F”, “07”→ “ 38”, “15”→ “2A”, and so on.
DATR[17:0]	Input/Output	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKR	Input/Output	Master and Slave cascade control signal.
DIOR	Input/Output	Master and Slave cascade control signal..
POLR	Input/Output	Master and Slave cascade control signal.
LDR	Input/Output	Master and Slave cascade control signal.
SYNCR	Input/Output	Master and Slave cascade control signal.
DATL[17:0]	Input/Output	Multi function I/O pin. Refer to the Cascade DAT pin mapping table for the detail.
DCLKL	Input/Output	Master and Slave cascade control signal.
DIOL	Input/Output	Master and Slave cascade control signal.
POLL	Input/Output	Master and Slave cascade control signal.
LDL	Input/Output	Master and Slave cascade control signal.
SYNCL	Input/Output	Master and Slave cascade control signal.
VDDA	Power Input	Power supply for analog circuits
VSSA	Power Input	Ground pins for analog circuits
VDD	Power Input	Power supply for digital circuits
VSS	Power Input	Ground pins for digital circuits
SO1~SO1200	Output	Source Driver Output Signals. All outputs will be of unknown values under stand-by mode.
ALIGN	Mark	For assembly alignment.

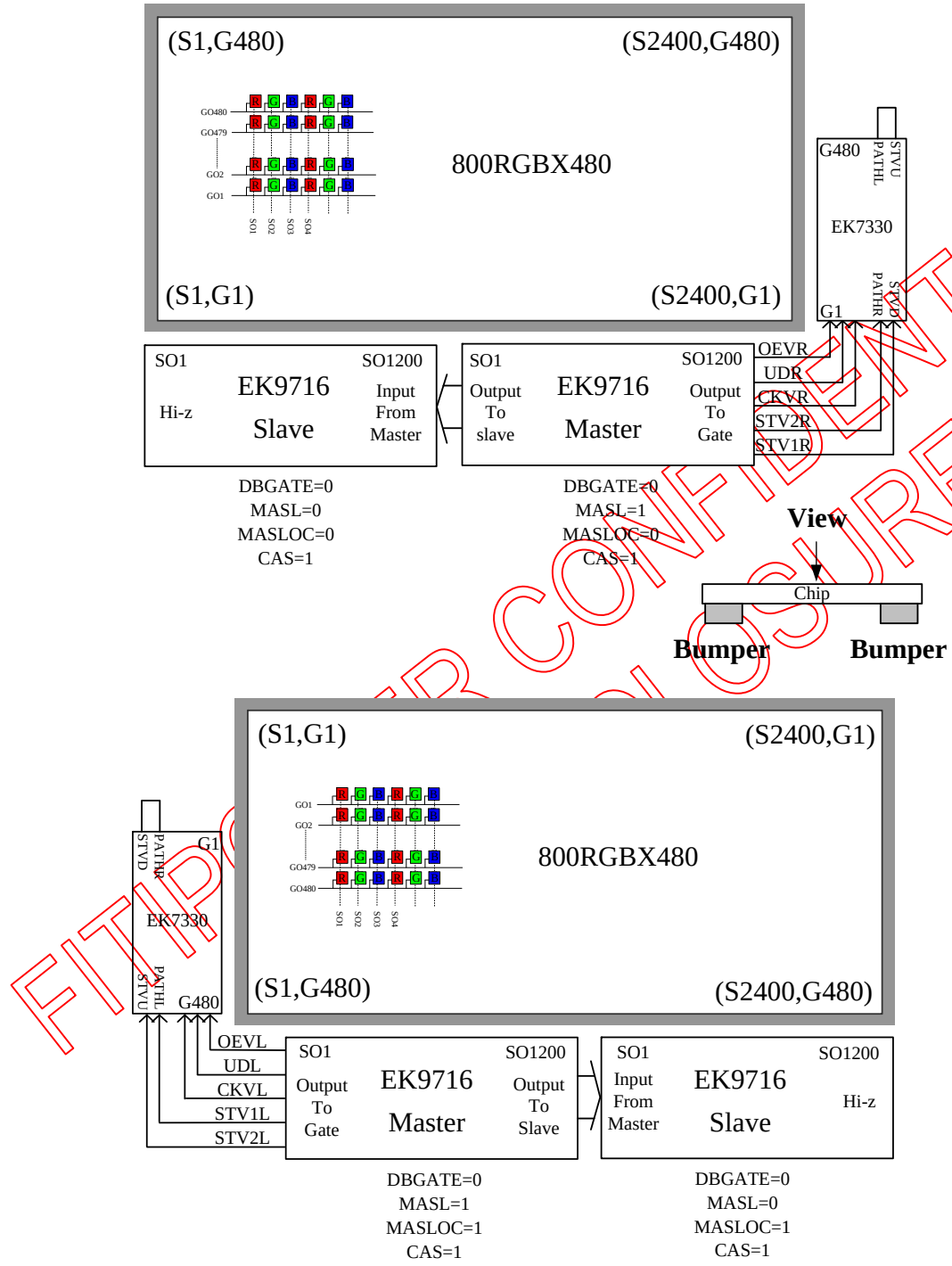
Pin Name	Pin Type	Description
COM_PASSR COM_PASSL	Shorted line	Internal link together between input side and output side.
COM1_T COM2_T	Shorted line	Internal link together between input side and output side.
TP17~0	Testing	Float these pins for normal operation.
SHIELDING	Shielding	IC Shielding pads. Those pins are internally connected to the VSSA. DO NOT connect to any WOA on the panel.
DASHD	Shielding	Data Bus Shielding pad. Those pins are internally connected to the VSS. RECOMMAND to add shielding lines on the FPC to reduce EMI.

EK9716 Pass Line Description:

Pass Line No:	Pad Name	
1	COM_PASSR	COM1_T
2	COM_PASSL	COM2_T

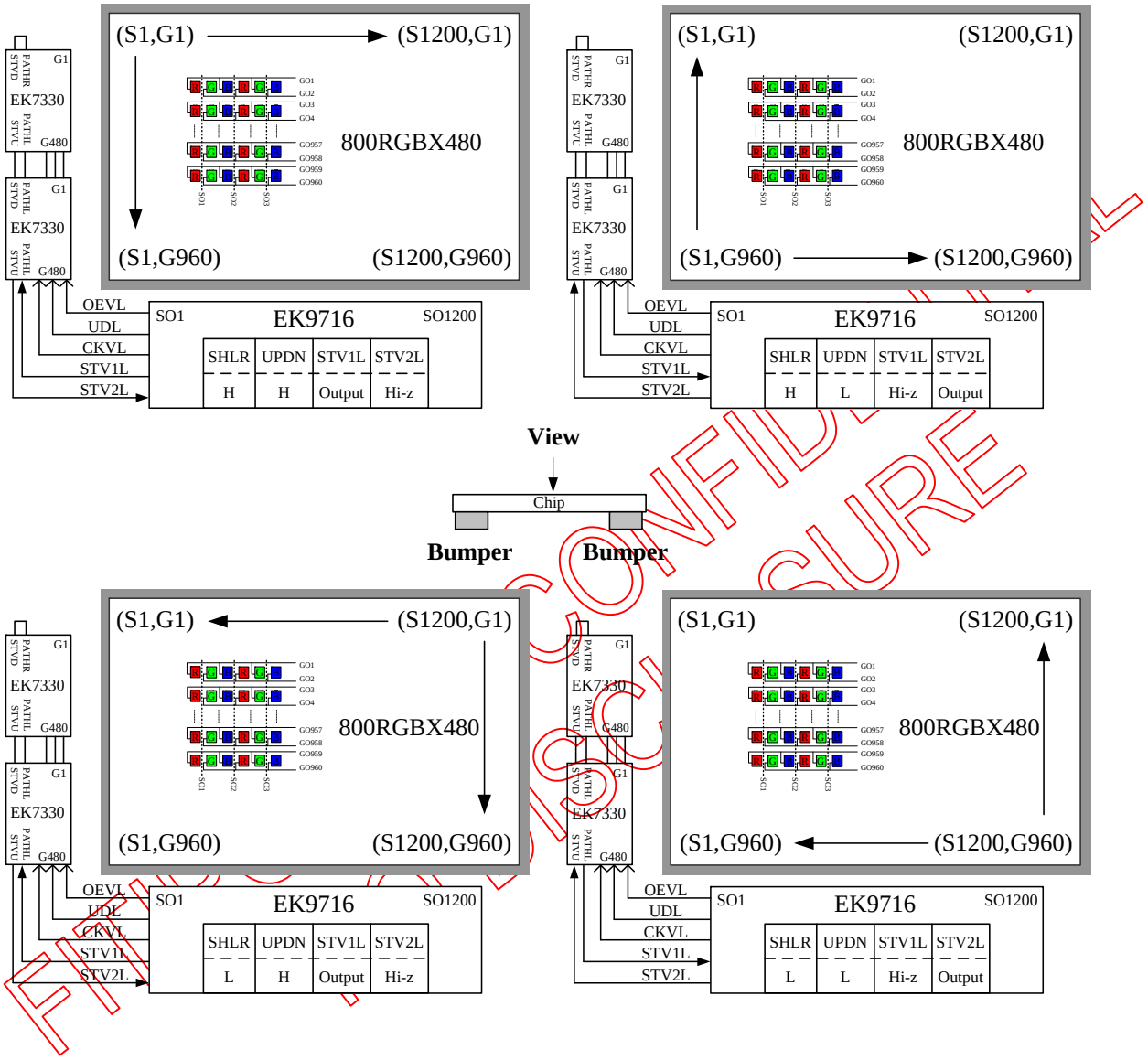
4.1. Chip Driver configuration examples of the EK9716

Two pieces of EK9716 driver are cascaded application for 800RGB x480



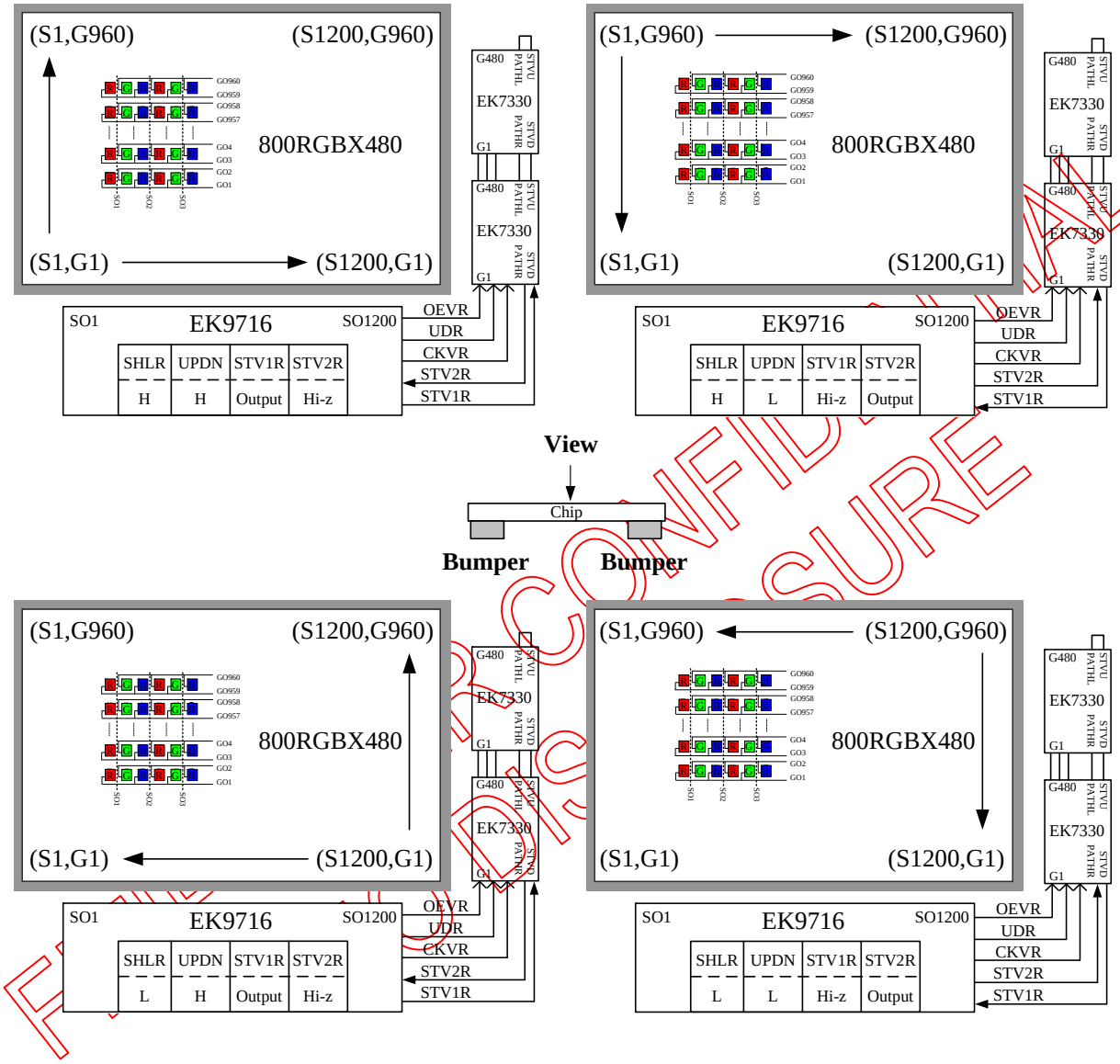
4.2. EK9716 put down and EK7330 put left side for 800RGBx480 of dual-gate mode

When DBGATE=1, MASL=1, MASLOC=X and CAS=0, application of the EK9716 will be illustrated as figure.



4.3. EK9716 put down and EK7330 put right side for 800RGBx480 of dual-gate mode

When DBGATE=1, MASL=1, MASLOC=X and CAS=0, application of the EK9716 will be illustrated as figure.



4.4. Value of wiring resistance to each pin

The recommended wiring resistance values are shown below. The wiring resistance values affect the current capacity of the power supply, so be sure to design using values that do not exceed those recommended.

wiring resistance

Pin Name	Wiring resistance value(Ω)	Pin Name	Wiring resistance value (Ω)
VDD	<25	BIST	<1K
VDDA	<5	CAS	<1K
VSS	<25	CABC_EN[1:0]	<1K
VSSA	<5	CSB/SCL/SDA	<200
GMAV1~GMAV14	<10	DATR[17:0]	<200 & 20 pf
DR[07:00]	<200	DCLKR	<200 & 20 pf
DG[07:00]	<200	DIOR	<200 & 20 pf
DB[07:00]	<200	POLR	<200 & 20 pf
DEN	<200	LDR	<200 & 20 pf
MODE	<1K	SYNCR	<200 & 20 pf
RES[1:0]	<1K	DATL[17:0]	<200 & 20 pf
DITHB	<1K	DCLKL	<200 & 20 pf
CLKPOL	<1K	DIOL	<200 & 20 pf
DIMO	<1K	POLL	<200 & 20 pf
CFSEL	<1K	LDL	<200 & 20 pf
DBGATE	<1K	CASCADE GMAV1~GMAV14	<30
RSTB	<1K	CLKIN	<50
MASL	<1K	HSD	<200
MASLOC	<1K	VSD	<200
SHLR	<1K		
UPDN	<1K		

DATR[17:0] / DATL[17:0] pin mapping Table:

DATR[17:0]	DBGATE = “0” MASL = “1” MASLOC = “0” CAS = “1”	DBGATE = “0” MASL = “1” MASLOC = “1” CAS = “1”	DBGATE = “0” MASL = “0” MASLOC = “0” CAS = “1”	DBGATE = “0” MASL = “0” MASLOC = “1” CAS = “1”	DBGATE = “1” MASL = “1” MASLOC = “X” CAS = “0”	DBGATE = “0” MASL = “1” MASLOC = “X” RES[1:0]=”1X” CAS = “0”
Description	Master for cascade. Master locate on panel right side	Master for cascade. Master locate on panel left side	Slave for cascade. Master locate on panel right side	Slave for cascade. Master locate on panel left side	Dual Gate Mode	Single Source Mode
DATR0	X	DAT0	DAT0	X	X	X
DATR1	X	DAT1	DAT1	X	X	X
DATR2	OEV	DAT2	DAT2	X	OEV	OEV
DATR3	X	DAT3	DAT3	X	X	X
DATR4	UD	DAT4	DAT4	X	UD	UD
DATR5	X	DAT5	DAT5	X	X	X
DATR6	CKV	DAT6	DAT6	X	CKV	CKV
DATR7	X	DAT7	DAT7	X	X	X
DATR8	STV1	DAT8	DAT8	X	STV1	STV1
DATR9	X	DAT9	DAT9	X	X	X
DATR10	STV2	DAT10	DAT10	X	STV2	STV2
DATR11	X	DAT11	DAT11	X	X	X
DATR12	STV1	DAT12	DAT12	X	STV1	STV1
DATR13	X	DAT13	DAT13	X	X	X
DATR14	X	DAT14	DAT14	X	X	X
DATR15	X	DAT15	DAT15	X	X	X
DATR16	STBN	DAT16	DAT16	X	STBN	STBN
DATR17	X	DAT17	DAT17	X	X	X
DCLKR	X	DCLK	DCLK	X	X	X
DIOR	X	DIO	DIO	X	X	X
LDR	X	LD	LD	X	X	X
SYNCR	X	SYNC	SYNC	X	X	X
DATL0	DAT0	X	X	DAT0	X	X
DATL1	DAT1	X	X	DAT1	X	X
DATL2	DAT2	OEV	X	DAT2	OEV	OEV
DATL3	DAT3	X	X	DAT3	X	X
DATL4	DAT4	UD	X	DAT4	UD	UD
DATL5	DAT5	X	X	DAT5	X	X
DATL6	DAT6	CKV	X	DAT6	CKV	CKV
DATL7	DAT7	X	X	DAT7	X	X
DATL8	DAT8	STV1	X	DAT8	STV1	STV1
DATL9	DAT9	X	X	DAT9	X	X
DATL10	DAT10	STV2	X	DAT10	STV2	STV2
DATL11	DAT11	X	X	DAT11	X	X
DATL12	DAT12	STV1	X	DAT12	STV1	STV1
DATL13	DAT13	X	X	DAT13	X	X
DATL14	DAT14	X	X	DAT14	X	X
DATL15	DAT15	X	X	DAT15	X	X
DATL16	DAT16	STBN	X	DAT16	STBN	STBN
DATL17	DAT17	X	X	DAT17	X	X
DCLKL	DCLK	X	X	DCLK	X	X
DIOL	DIO	X	X	DIO	X	X
LDL	LD	X	X	LD	X	X
SYNCL	SYNC	X	X	SYNC	X	X

5. 3-WIRE SERIAL PORT INTERFACE

5.1. 3-Wire Command Format

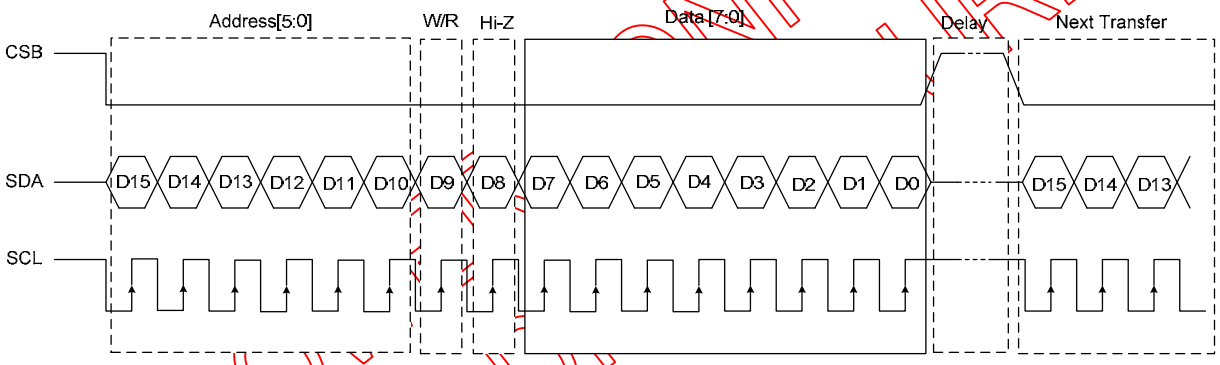
EK9716 use the 3-wire serial port as communication interface for all the function and parameter setting.

3-Wire communication can be bi-directional controlled by the “R/W” bit in address field. EK9716 3-Wire engine act as a “slave mode” for all the time, and will not issue any command to the 3-Wire bus itself.

Under read mode, 3-Wire engine will return the data during “Data phase”. The returned data should be latched at the rising edge of SCL by external controller. Data in the “Hi-Z phase” will be ignored by 3-Wire engine during write operation, and should be ignored during read operation also. During read operation, external controller should float SDA pin under “Hi-Z phase” and “Data phase”.

Each Read/Write operation should be exactly 16 bit. To prevent from incorrect setting of the internal register, any write operation with more or less than 16 bit data during a CSB Low period will be ignored by 3-Wire engine.

For prevent from incorrect setting of the internal register. Please refer to the section of “3-Wire Timing Diagram” for the detail timing.



3-Wire timing chart

3-Wire Command Format

Bit	Description
D15 – D10	Register Address [5:0].
D9	W/R control bit. “0” for Write; “1” for Read
D8	Hi-Z bit during read mode. Any data within this bits will be ignored during write mode
D7 – D0	Data for the W/R operation to the address indicated by Address phase

3-Wire Writer Format

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						0	X	DATA (Issue by external controller)							

3-Wire Read Format

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register Address [5:0]						1	Hi-Z	DATA (Issue by 3-Wire engine)							

5.2. 3-Wire Control Registers

Following table list all the 3-Wire control registers and bit name definition for EK9716. Refer to the next section for detail register function description, please.

Setting of all the 3-Wire registers will take effect at the coming falling edge of VSD except GRB and STB bit.

5.3. 3-Wire Control Register List

NO.	Address						R/W	D8	MSB	Initial value						LSB
	D15	D14	D13	D12	D11	D10	D9		D7	D6	D5	D4	D3	D2	D1	D0
R0	0	0	0	0	0	0	R/W(0)	X	RES[1]	RES[0]	SHLR	UPDN	STBYB	GRB	DCLKP	MODE
									0	0	1	0	1	1	0	1
R1	0	0	0	0	0	1	R/W(0)	X	NBWB	CFSEL	SCI_ON	CABC_EN[1]	CABC_EN[0]	HFRC	DITHB	BIST
									1	1	0	0	0	1	1	0

Note:
1. The register except upper list was for testing use, to write test register was not allowed.

R0: System Control Register

Designation	Address	Description
MODE	R0[0]	DE / SYNC mode select. MODE="0", HSD/VSD mode. MODE="1", DE mode. (Default)
DCLKPOL	R0[1]	DCLK polarity control bit. DCLKPOL="0": Data sampling at DCLK falling edge. (Default) DCLKPOL="1": Data sampling at DCLK rising edge.
GRB	R0[2]	Global reset bit. GRB="0", The controller is in reset state. GRB="1", Normal operation. (Default)
STBYB	R0[3]	Standby mode selection bit. STBYB="0", Timing control and driver are off. All outputs are High-Z. STBYB="1", Normal operation. (Default)
UPDN	R0[4]	G Gate Up or Down scan control. UPDN = "0", STV2 output vertical start pulse and UD pin output logical "0" to Gate driver. (Default) UPDN = "1", STV1 output vertical start pulse and UD pin output logical "1" to Gate driver.
SHLR	R0[5]	Right/Left sequence control of source driver. SHLR="0", Shift left: Last data=S1<-S2<-S3 … <-S1200=First data. SHLR="1", Shift right: First data=S1->S2->S3 … ->S1200=Last data. (Default)
RES[1:0]	R0[7:6]	Display resolution selection. RES[1:0] = "00", for 800(RGB)*480 display resolution.(Default) RES[1:0] = "01", for 800(RGB)*600 display resolution. RES[1:0] = "10", for 400(RGB)*480 display resolution. RES[1:0] = "11", for 400(RGB)*240 display resolution.

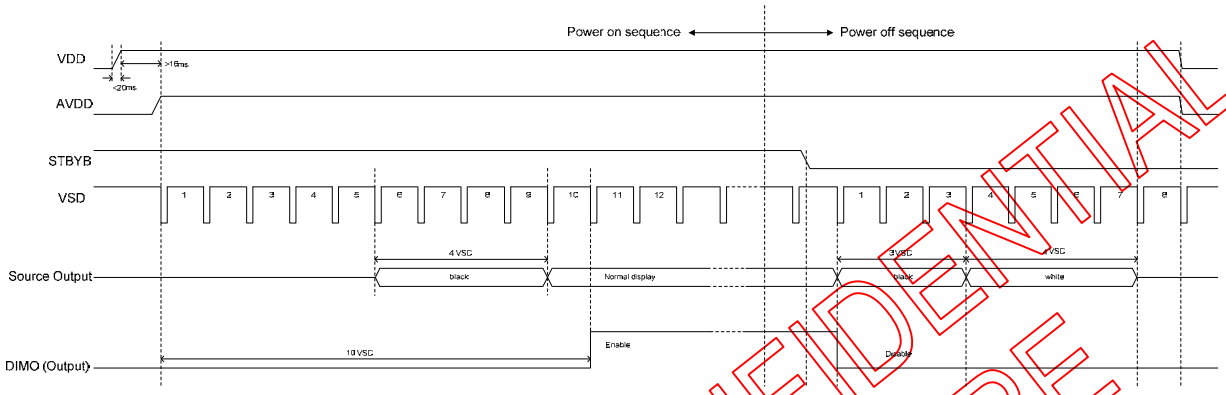
R1: System Control Register

Designation	Address	Description
BIST	R1[0]	Normal Operation/BIST pattern select. BIST = “0” : Normal Operation (Default) BIST = “1” : BIST(DCLK input is not needed)
DITHB	R1[1]	Dithering function enable control. Normally pull high DITHB = “0”, Enable internal dithering function. DITHB = “1”, Disable internal dithering function.(Default)
HFRC	R1[2]	H-FRC selection. HFRC = “0” : FRC enable. (Default) HFRC = “1” : HiFRC enable. If DITHER = “0” , disable dithering function(HiFRC and FRC disable)
CABC_EN[1:0]	R1[4:3]	CABC H/W enable pin. Normally pull low. When CABC_EN=”00”, CABC OFF. (Default mode) When CABC_EN=”01”, User interface Image. When CABC_EN=”10”, Still Picture. When CABC_EN=”11”, Moving Image.
SCI_ON	R1[5]	Enable 3-wire control function. Normally pull low SCI_ON = “0” : Base on pin control function. (Default) SCI_ON = “1” : Base on 3-wire register.
CFSEL	R1[6]	Color Filter type selection. Normally pull high CFSEL = “0”, Delta mode CFSEL = “1”, Stripe mode. (Default)
NBWB	R1[7]	Normally black or normally white setting. NBWB = “0” : Normally black NBWB = “1” : Normally white (Default)

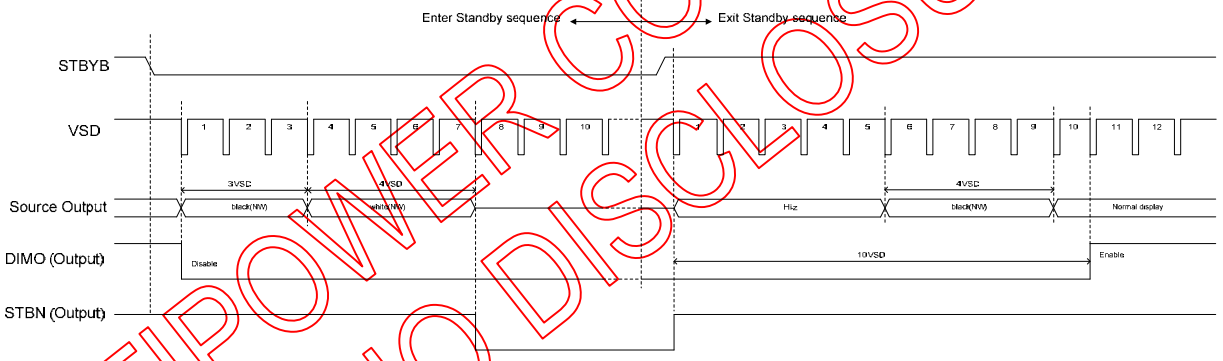
6. FUNCTION DESCRIPTION

6.1. Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (T_{POR}) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.



Power-On/Off Timing Sequence



Enter and Exit Standby Mode Sequence

6.2. Input Data VS Output Channels

6.2.1. DBGATE="0", CFSEL="1", Stripe Mode

SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]

SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]

6.2.2. DBGATE="0", CFSEL="0", Delta Mode

SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DG[07:00]	DB[07:00]	DR[07:00]	---	DG[07:00]	DB[07:00]	DR[07:00]

SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line	DR[07:00]	DG[07:00]	DB[07:00]	---	DR[07:00]	DG[07:00]	DB[07:00]
Even Line	DG[07:00]	DB[07:00]	DR[07:00]	---	DG[07:00]	DB[07:00]	DR[07:00]

6.2.3. DBGATE="1", CFSEL="1", Stripe Mode

SHLR="1" , right shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]		DR[07:00]	DB[07:00]	DG[07:00]
Even Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]	---	DG[07:00]	DR[07:00]	DB[07:00]

SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]		DR[07:00]	DB[07:00]	DG[07:00]
Even Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]	---	DG[07:00]	DR[07:00]	DB[07:00]

6.2.4. DBGATE="1", CFSEL="0", Delta Mode

SHLR="1" , right shift

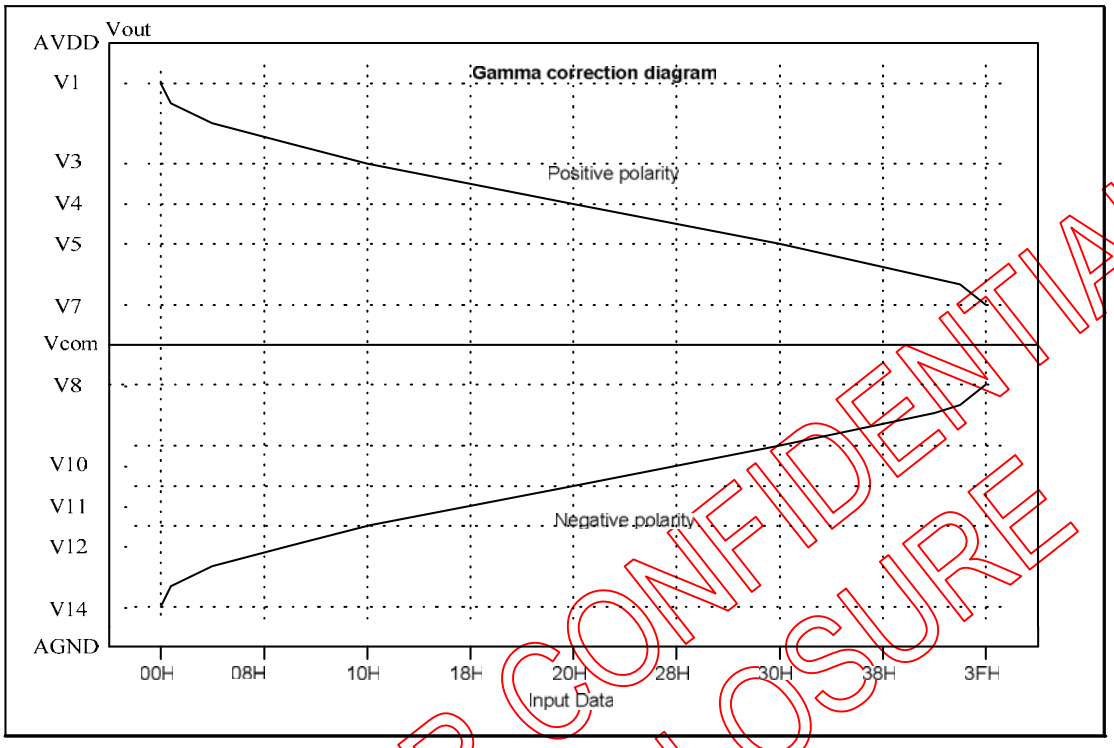
Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	First data			→	Last data		
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn+1	DB[07:00]	DG[07:00]	DR[07:00]	---	DB[07:00]	DG[07:00]	DR[07:00]

SHLR="0", left shift

Output	SO1	SO2	SO3	---	SO1198	SO1199	SO1200
Order	Last data			←	First data		
Odd Line/Gn	DR[07:00]	DB[07:00]	DG[07:00]	---	DR[07:00]	DB[07:00]	DG[07:00]
Odd Line/Gn+1	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn	DG[07:00]	DR[07:00]	DB[07:00]		DG[07:00]	DR[07:00]	DB[07:00]
Even Line/Gn+1	DB[07:00]	DG[07:00]	DR[07:00]	---	DB[07:00]	DG[07:00]	DR[07:00]

6.3. Input Data VS Output Voltage

The figure below shows the relationship between the input data and the output voltage. Refer to the following pages for the relative resistor values and voltage calculation method.



Remark:
Dual Gate：VDDA-0.1V > V1 > V3 > V4 > V5 > V7; V8 > V10 > V11 > V12 > V14 > VSSA+0.1V
Cascade：VDDA-1V > V1 > V3 > V4 > V5 > V7; V8 > V10 > V11 > V12 > V14 > VSSA+1V

6.4. Input Data and Output Voltage Reference Table

Gamma correction resistor ratio

Name	Resistor	Name	Resistor
R0	8.0	R32	0.63
R1	7.11	R33	0.63
R2	6.22	R34	0.63
R3	5.33	R35	0.62
R4	4.45	R36	0.62
R5	3.56	R37	0.62
R6	2.97	R38	0.62
R7	2.48	R39	0.61
R8	2.14	R40	0.61
R9	1.89	R41	0.61
R10	1.69	R42	0.62
R11	1.54	R43	0.63
R12	1.39	R44	0.64
R13	1.28	R45	0.64
R14	1.21	R46	0.65
R15	1.14	R47	0.67
R16	1.05	R48	0.75
R17	1	R49	0.9
R18	0.94	R50	1
R19	0.91	R51	1
R20	0.87	R52	1.2
R21	0.84	R53	1.2
R22	0.81	R54	1.4
R23	0.78	R55	1.5
R24	0.76	R56	1.7
R25	0.73	R57	2
R26	0.71	R58	2.1
R27	0.7	R59	2.3
R28	0.68	R60	3.1
R29	0.67	R61	4.2
R30	0.66	R62	20.1
R31	0.64		

V1, V14 → R0

V4, V11 ← R32

V3, V12 → R15

V5, V10 ← R47

V7, V8 ← R62

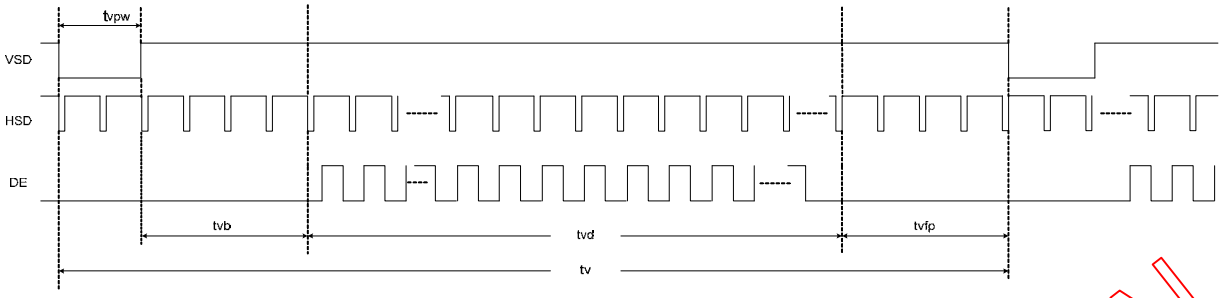
V4, V11 → R31

Output Voltage VS Input Data

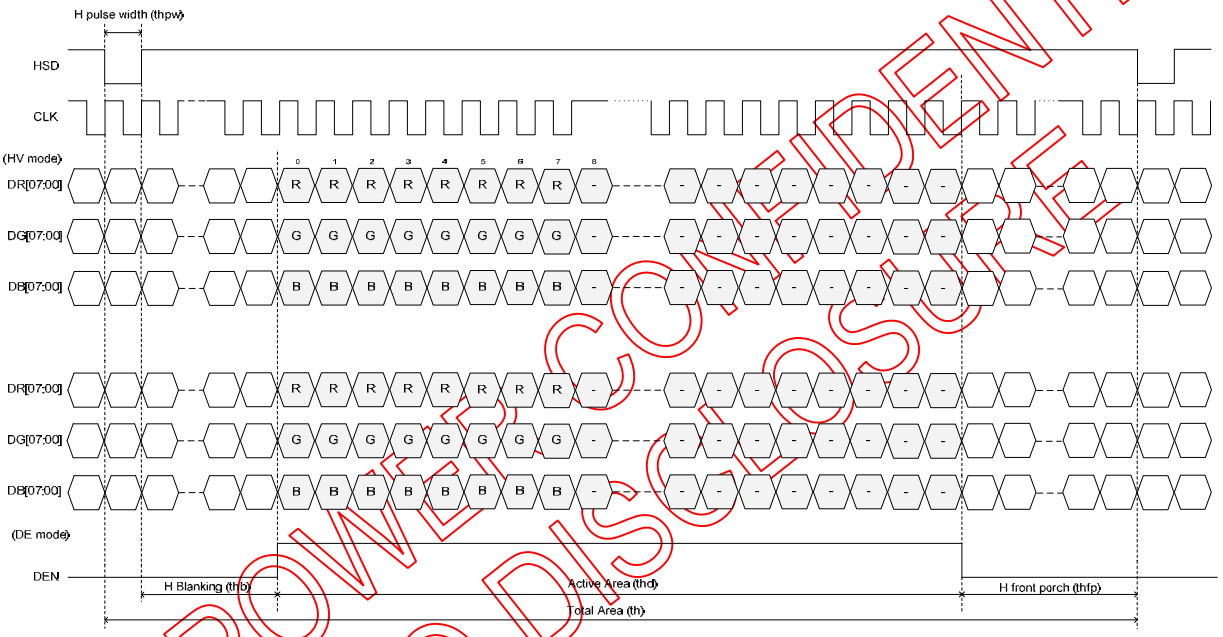
Data	Positive polarity Output Voltage	Negative polarity Output Voltage
00H	V1	V14
01H	V3 + (V1 – V3) X 44.4 / 52.4	V14+ (V12 – V14) X 8 / 52.4
02H	V3 + (V1 – V3) X 37.29 / 52.4	V14+ (V12 – V14) X 15.11 / 52.4
03H	V3 + (V1 – V3) X 31.06 / 52.4	V14+ (V12 – V14) X21.34 / 52.4
04H	V3 + (V1 – V3) X 25.73 / 52.4	V14+ (V12 – V14) X 26.67 / 52.4
05H	V3 + (V1 – V3) X 21.28 / 52.4	V14+ (V12 – V14) X 31.12 / 52.4
06H	V3 + (V1 – V3) X 17.73 / 52.4	V14+ (V12 – V14) X 34.67 / 52.4
07H	V3 + (V1 – V3) X 14.76 / 52.4	V14+ (V12 – V14) X 37.64 / 52.4
08H	V3 + (V1 – V3) X 12.28 / 52.4	V14+ (V12 – V14) X 40.11 / 52.4
09H	V3 + (V1 – V3) X 10.14 / 52.4	V14+ (V12 – V14) X 42.26 / 52.4
0AH	V3 + (V1 – V3) X 8.25 / 52.4	V14+ (V12 – V14) X 44.15 / 52.4
0BH	V3 + (V1 – V3) X 6.56 / 52.4	V14+ (V12 – V14) X 45.84 / 52.4
0CH	V3 + (V1 – V3) X 5.02 / 52.4	V14+ (V12 – V14) X 47.38 / 52.4
0DH	V3 + (V1 – V3) X 3.64 / 52.4	V14+ (V12 – V14) X 48.76 / 52.4
0EH	V3 + (V1 – V3) X 2.36 / 52.4	V14+ (V12 – V14) X 50.04 / 52.4
0FH	V3 + (V1 – V3) X 1.14 / 52.4	V14+ (V12 – V14) X 51.26 / 52.4
10H	V3	V12
11H	V4 + (V3 – V4) X 11.7 / 12.75	V12 + (V11 – V12) X 1.05 / 12.75
12H	V4 + (V3 – V4) X 10.7 / 12.75	V12 + (V11 – V12) X 2.05 / 12.75
13H	V4 + (V3 – V4) X 9.76 / 12.75	V12 + (V11 – V12) X 2.99 / 12.75
14H	V4 + (V3 – V4) X 8.85 / 12.75	V12 + (V11 – V12) X 3.9 / 12.75
15H	V4 + (V3 – V4) X 7.98 / 12.75	V12 + (V11 – V12) X 4.77 / 12.75
16H	V4 + (V3 – V4) X 7.14 / 12.75	V12 + (V11 – V12) X 5.61 / 12.75
17H	V4 + (V3 – V4) X 6.33 / 12.75	V12 + (V11 – V12) X 6.41 / 12.75
18H	V4 + (V3 – V4) X 5.55 / 12.75	V12 + (V11 – V12) X 7.19 / 12.75
19H	V4 + (V3 – V4) X 4.8 / 12.75	V12 + (V11 – V12) X 7.95 / 12.75
1AH	V4 + (V3 – V4) X 4.06 / 12.75	V12 + (V11 – V12) X 8.68 / 12.75
1BH	V4 + (V3 – V4) X 3.35 / 12.75	V12 + (V11 – V12) X 9.4 / 12.75
1CH	V4 + (V3 – V4) X 2.65 / 12.75	V12 + (V11 – V12) X10.09/ 12.75
1DH	V4 + (V3 – V4) X 1.97 / 12.75	V12 + (V11 – V12) X10.78/ 12.75
1EH	V4 + (V3 – V4) X 1.3 / 12.75	V12 + (V11 – V12) X11.44/ 12.75
1FH	V4 + (V3 – V4) X 0.65 / 12.75	V12 + (V11 – V12) X 12.1 / 12.75

Data	Positive polarity Output Voltage	Negative polarity Output Voltage
20H	V4	V11
21H	V5 + (V4 – V5) X 9.37 / 10	V11 + (V10 – V11) X 0.63 / 10
22H	V5 + (V4 – V5) X 8.74 / 10	V11 + (V10 – V11) X 1.26 / 10
23H	V5 + (V4 – V5) X 8.11 / 10	V11 + (V10 – V11) X 1.89 / 10
24H	V5 + (V4 – V5) X 7.49 / 10	V11 + (V10 – V11) X 2.51 / 10
25H	V5 + (V4 – V5) X 6.87 / 10	V11 + (V10 – V11) X 3.13 / 10
26H	V5 + (V4 – V5) X 6.25 / 10	V11 + (V10 – V11) X 3.75 / 10
27H	V5 + (V4 – V5) X 5.63 / 10	V11 + (V10 – V11) X 4.36 / 10
28H	V5 + (V4 – V5) X 5.02 / 10	V11 + (V10 – V11) X 4.98 / 10
29H	V5 + (V4 – V5) X 4.41 / 10	V11 + (V10 – V11) X 5.59 / 10
2AH	V5 + (V4 – V5) X 3.8 / 10	V11 + (V10 – V11) X 6.2 / 10
2BH	V5 + (V4 – V5) X 3.18 / 10	V11 + (V10 – V11) X 6.82 / 10
2CH	V5 + (V4 – V5) X 2.55 / 10	V11 + (V10 – V11) X 7.45 / 10
2DH	V5 + (V4 – V5) X 1.91 / 10	V11 + (V10 – V11) X 8.08 / 10
2EH	V5 + (V4 – V5) X 1.27 / 10	V11 + (V10 – V11) X 8.72 / 10
2FH	V5 + (V4 – V5) X 0.62 / 10	V11 + (V10 – V11) X 9.38 / 10
30H	V5	V10
31H	V7 + (V5 – V7) X 43.7 / 44.45	V10 + (V8 – V10) X 0.75 / 44.45
32H	V7 + (V5 – V7) X 42.8 / 44.45	V10 + (V8 – V10) X 1.65 / 44.45
33H	V7 + (V5 – V7) X 41.8 / 44.45	V10 + (V8 – V10) X 2.65 / 44.45
34H	V7 + (V5 – V7) X 40.8 / 44.45	V10 + (V8 – V10) X 3.65 / 44.45
35H	V7 + (V5 – V7) X 39.6 / 44.45	V10 + (V8 – V10) X 4.85 / 44.45
36H	V7 + (V5 – V7) X 38.4 / 44.45	V10 + (V8 – V10) X 6.05 / 44.45
37H	V7 + (V5 – V7) X 37 / 44.45	V10 + (V8 – V10) X 7.45 / 44.45
38H	V7 + (V5 – V7) X 35.5 / 44.45	V10 + (V8 – V10) X 8.95 / 44.45
39H	V7 + (V5 – V7) X 33.8 / 44.45	V10 + (V8 – V10) X10.6 / 44.45
3AH	V7 + (V5 – V7) X 31.8 / 44.45	V10 + (V8 – V10) X 12 / 44.45
3BH	V7 + (V5 – V7) X 29.7/ 44.45	V10 + (V8 – V10) X 14.7 / 44.45
3CH	V7 + (V5 – V7) X 27.4 / 44.45	V10 + (V8 – V10) X 17 / 44.45
3DH	V7 + (V5 – V7) X 24.3 / 44.45	V10 + (V8 – V10) X 20.1 / 44.45
3EH	V7 + (V5 – V7) X 20.1 / 44.45	V10 + (V8 – V10) X 24.3 / 44.45
3FH	V7	V8

6.5. Data Input Format



Vertical input timing



Horizontal input timing

6.6. Timing Characteristic

6.6.1. For 800 × 480 panel

Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		20	33.3	50	MHz	
1 Horizontal Line	th	908	928	1088	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	40	200		

Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd	480			H	
VSD period time	tv	517	525	712	H	tvpw+tvb=32H Is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	200	H	

6.6.2. For 800 × 600 panel

Horizontal input timing

Parameter	Symbol	Value			Unit	Note
Horizontal display area	thd	800			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		20	40	50	MHz	
1 Horizontal Line	th	908	1000	1088	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	112	200		

Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Vertical display area	tvd	600			H	
VSD period time	tv	644	660	839	H	tvpw+tvb=39H Is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	38	38	36	H	
VSD Front Porch	tvfp	5	21	200	H	

6.6.3. For 400 × 480 panel

Horizontal input timing

Parameter	Symbol	Value			Unit	
Horizontal display area	thd	400			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		1	16.4	50	MHz	
1 Horizontal Line	th	508	520	688	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	87		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	32	200		

Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Vertical display area	tvd	480			H	
VSD period time	tv	517	525	712	H	tvpw+tvb=32H Is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	31	31	29	H	
VSD Front Porch	tvfp	5	13	200	H	

6.6.4. For 400 × 240 panel

Horizontal input timing

Parameter	Symbol	Value			Unit	
Horizontal display area	thd	400			DCLK	
DCLK frequency	fclk	Min.	Typ.	Max		
		1	8.5	50	MHz	
1 Horizontal Line	th	508	520	688	DCLK	thb+thpw=88 DCLK is fixed.
HSD pulse width	thpw	1	48	47		
HSD Back Porch (Blanking)	thb	87	40	1		
HSD Front Porch	thfp	20	32	200		

Vertical input timing

Parameter	Symbol	Min.	Typ.	Max.	Unit	
Vertical display area	tvd	240			H	
VSD period time	tv	262	270	457	H	tvpw+tvb=17H Is fixed
VSD pulse width	tvpw	1	1	3	H	
VSD Back Porch (Blanking)	tvb	16	16	14	H	
VSD Front Porch	tvfp	5	13	200	H	

7. ELECTRICAL SPECIFICATION

7.1. Absolute Maximum Ratings

VOLTAGE (TA = 25°C, VSS = VSSA = 0V)

	Min.	Max.	Unit
Digital Supply Voltage, VDD	-0.5	+5.0	V
Analog Supply Voltage, VDDA, V1~V14	-0.5	+15.0	V

TEMPERATURE

	Min.	Max.	Unit
Operating temperature	-20	+85	°C
Storage temperature	-55	+125	°C

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposed to absolute maximum rating conditions for extended periods may affect device reliability.

7.2. Recommended Operating Range

Recommended Operating Range (TA = -20 to 85°C, VSS = VSSA = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital supply voltage	VDD	2.7	3.3	3.6	V
Analog supply voltage	VDDA	6.5	-	13.5	V
Digital input voltage	VIN	0	-	VDD	V

7.3. DC Characteristics

DC Characteristics

(TA = -20 to 85°C, VDD = 2.7 to 3.6V, VDDA = 6.5 to 13.5V, VSS = VSSA = 0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VDD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	μA
High level output voltage	Voh	Ioh= -400 μA	VDD-0.4	-	-	V
Low level output voltage	Vol	Iol= +400 μA	-	-	VSS+0.4	V
Pull low/high resistor	Ri	For the digital input pin @ VDD=3.3V	200K	250K	300K	ohm
Digital Operation current	Idd	Fclk=50 MHz, FLD=48KHz, VDD=3.3V	-	14	18	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	μA
Analog Operating Current	Idda	No load, Fclk=50MHz, FLD=48KHz @ VDDA=10V,V1=8V, V14=0.4V	-	7	12	mA
Analog Stand-by current	Ist2	No load, Clock and all functions are stopped	-	10	50	μA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input(Cascade Mode)	0.4*VDDA	-	VDDA-1	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input(Cascade Mode)	VSSA+1	-	0.6*VDDA	V
Input level of V1 ~ V7	Vref3	Gamma correction voltage input(Dual Gate Mode)	0.4*VDDA	-	VDDA-0.1	V
Input level of V8 ~ V14	Vref4	Gamma correction voltage input(Dual Gate Mode)	VSSA+0.1	-	0.6*VDDA	V
Output Voltage deviation	Vod1	Vo = VSSA+0.1V ~ VSSA+0.5V and Vo = VDDA-0.5V ~ VDDA-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = VSSA+0.5V ~ VDDA-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = VSSA+0.5V ~ VDDA-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ SO1200	0.1	-	VDDA-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ SO1200; Vo=0.1V v.s 1.0V , VDDA=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ SO1200; Vo=13.4V v.s 12.5V , VDDA=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7*Rn	1.0*Rn	1.3*Rn	ohm

7.4. AC Characteristics

AC Characteristics

(TA = -20 to 85°C, VDD = 2.7 to 3.6V, VDDA = 6.5 to 13.5V, VSS = VSSA = 0V)

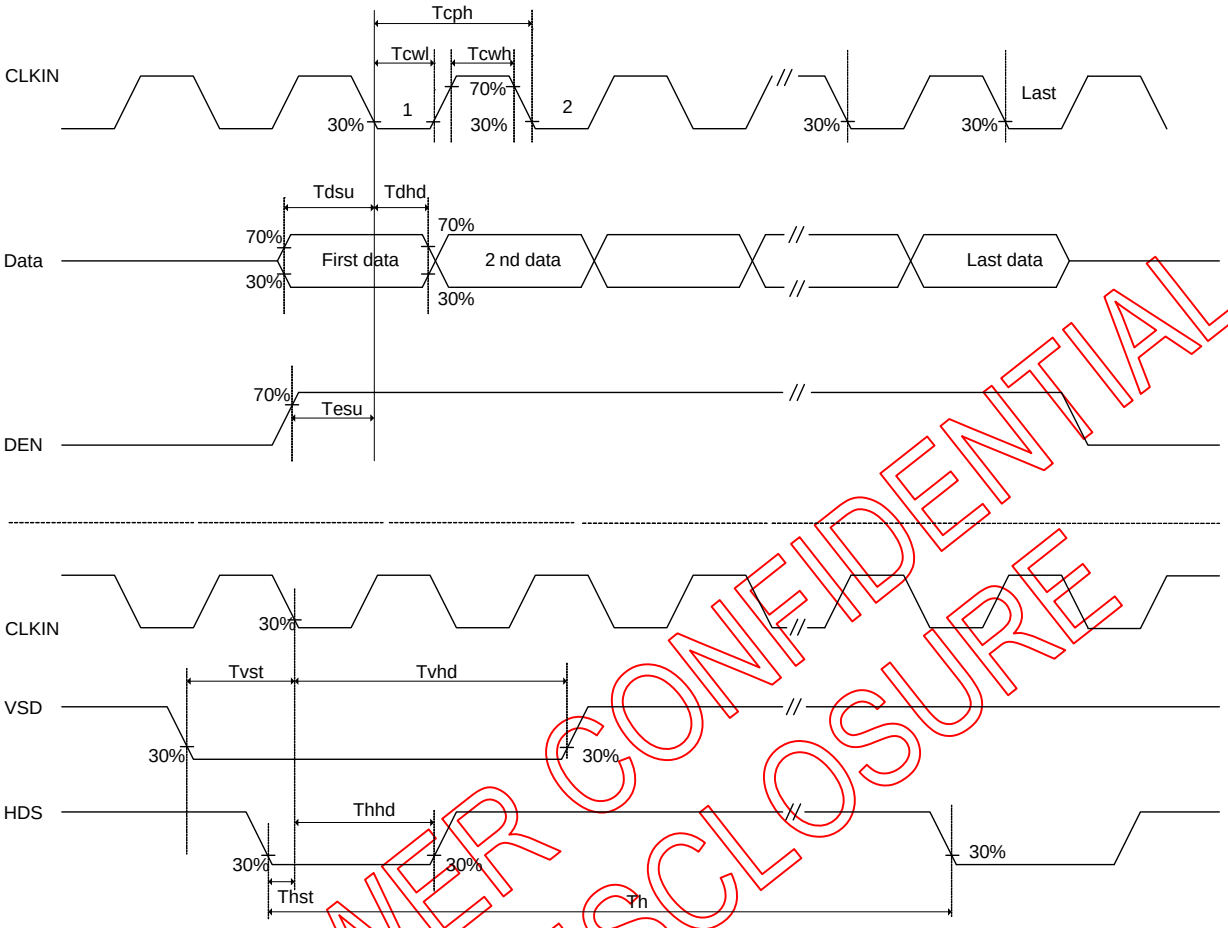
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
VDD Power On Slew rate	T_{POR}	From 0V to 90% VDD	-	-	20	ms
RSTB pulse width	T_{RST}	CLKIN = 50MHz	50	-	-	us
CLKIN cycle time	Tcph	-	20	-	-	ns
CLKIN pulse duty	Tcwh	-	40	50	60	%
VSD setup time	Tvst	-	8	-	-	ns
VSD hold time	Tvhd	-	8	-	-	ns
HSD setup time	Thst	-	8	-	-	ns
HSD hold time	Thhd	-	8	-	-	ns
Data set-up time	Tdsu	DR[7:0], DG[7:0], DB[7:0] to CLKIN	8	-	-	ns
Data hold time	Tdhd	DR[7:0], DG[7:0], DB[7:0] to CLKIN	8	-	-	ns
DEN setup time	Tesu	-	8	-	-	ns
DEN hold time	Tehd	-	8	-	-	ns
Output stable time	Tsst	10% to 90% target voltage, CL=120pF, R=10K ohm	-	-	6	us

7.5. Timing Table

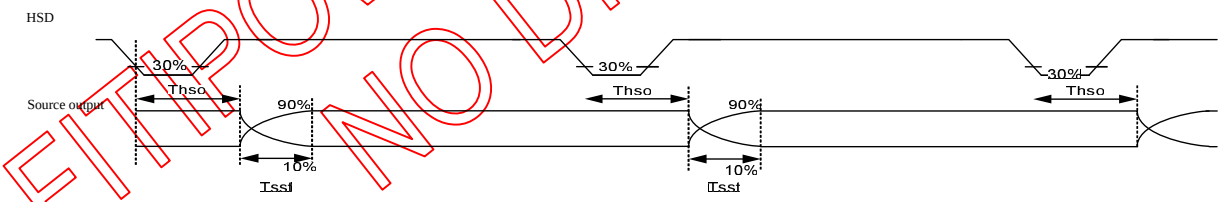
Parallel 24-bit RGB Mode

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKIN Frequency	Fclk	VDD = 3.0V ~3.6V	-	40	50	MHz
CLKIN Cycle Time	Tclk	-	20	25	-	ns
CLKIN Pulse Duty	Tcwh	Tclk	40	50	60	%
Time from HSD to Source Output	Thso	-	-	46	-	CLKIN
Time from HSD to LD	Thld	-	-	46	-	CLKIN
Time from HSD to STV	Thstv	-	-	2	-	CLKIN
Time from HSD to CKV	Thckv	-	-	20	-	CLKIN
Time from HSD to OEV	Thoev	-	-	4	-	CLKIN
LD Pulse W idth	Twld			10		CLKIN
CKV Pulse Width	Twckv	-	-	66	-	CLKIN
OEV Pulse Width	Twoev	-	-	74	-	CLKIN

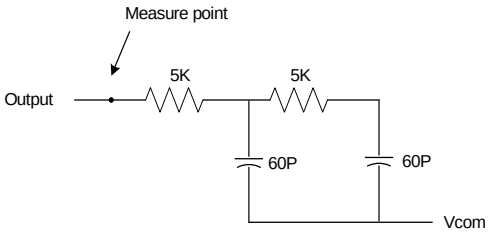
7.6. Timing Waveform



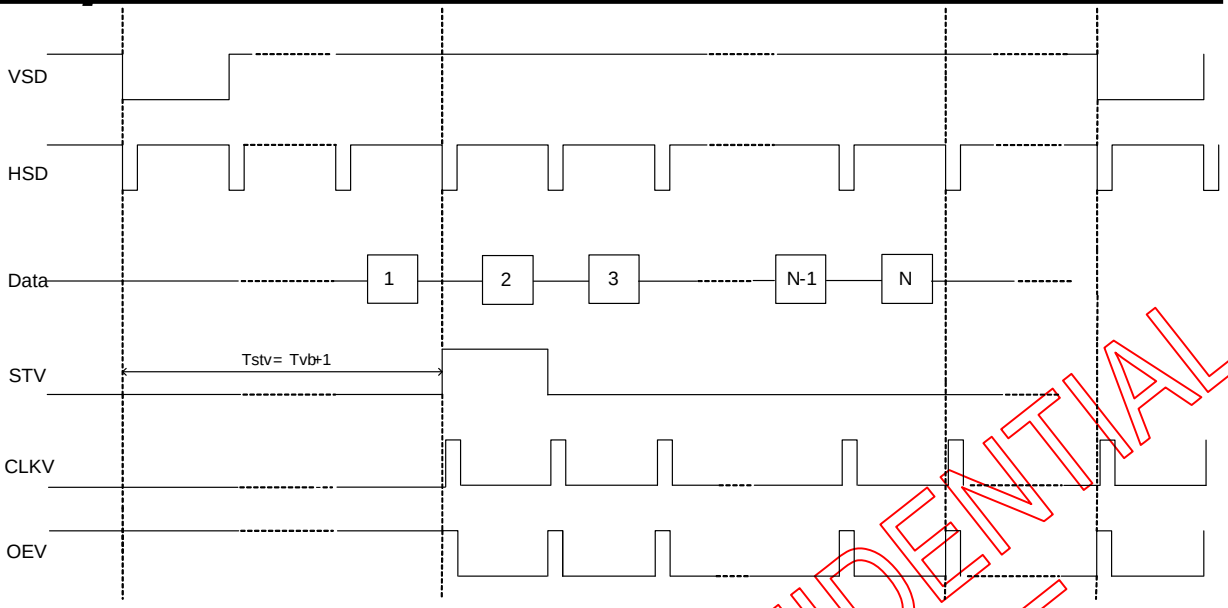
Input Clock and Data Timing Diagram



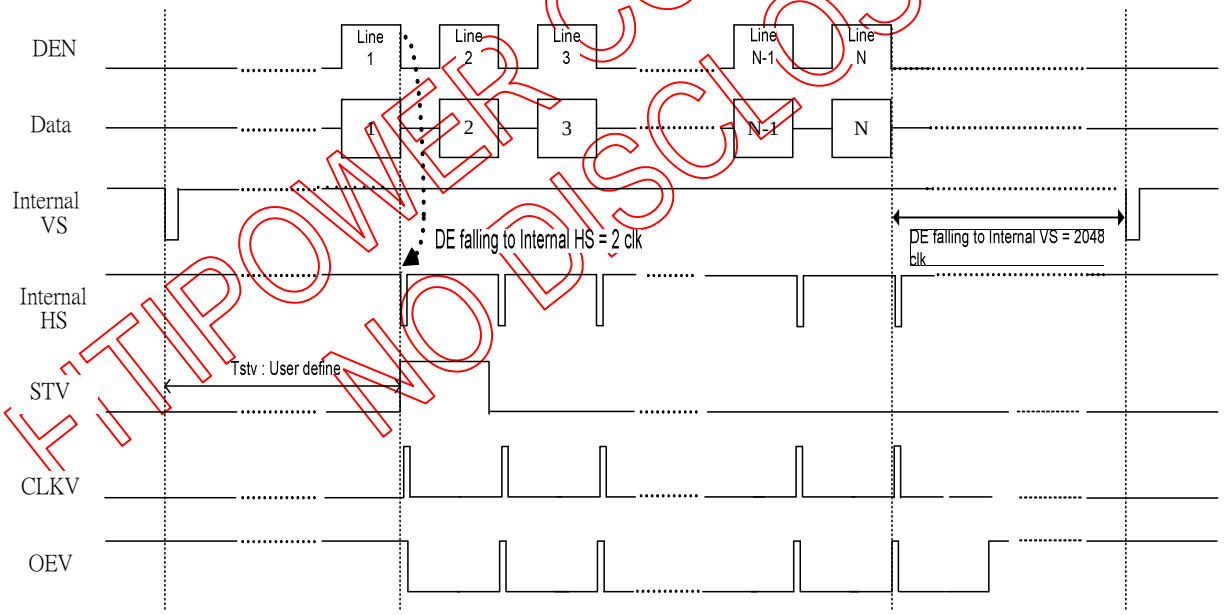
Source Output Timing Diagram(Cascade)



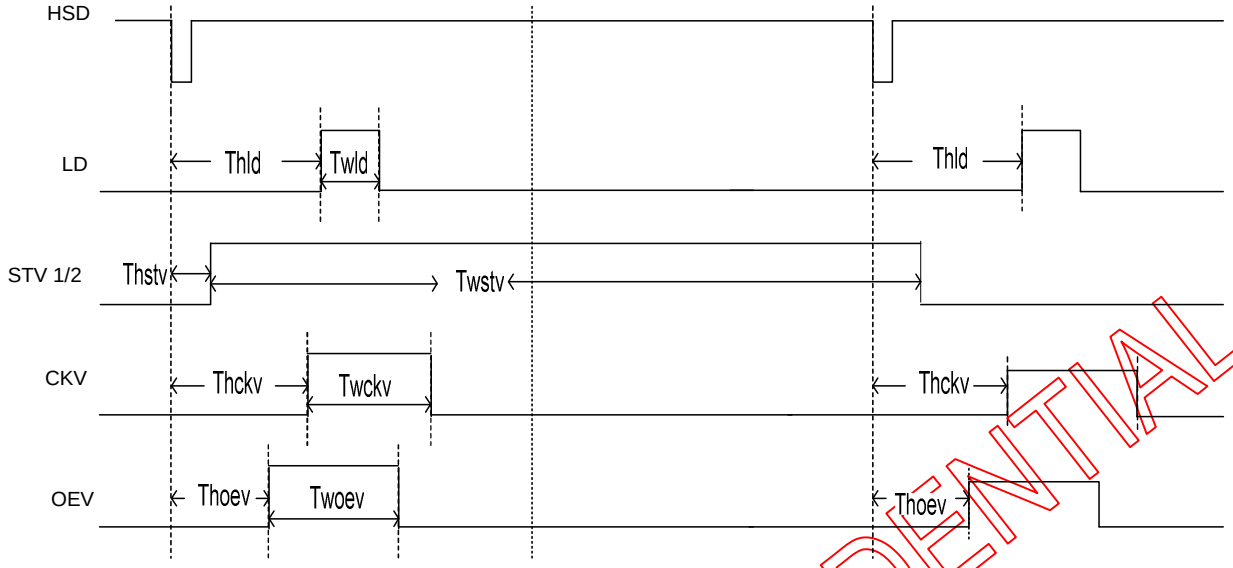
Output load condition



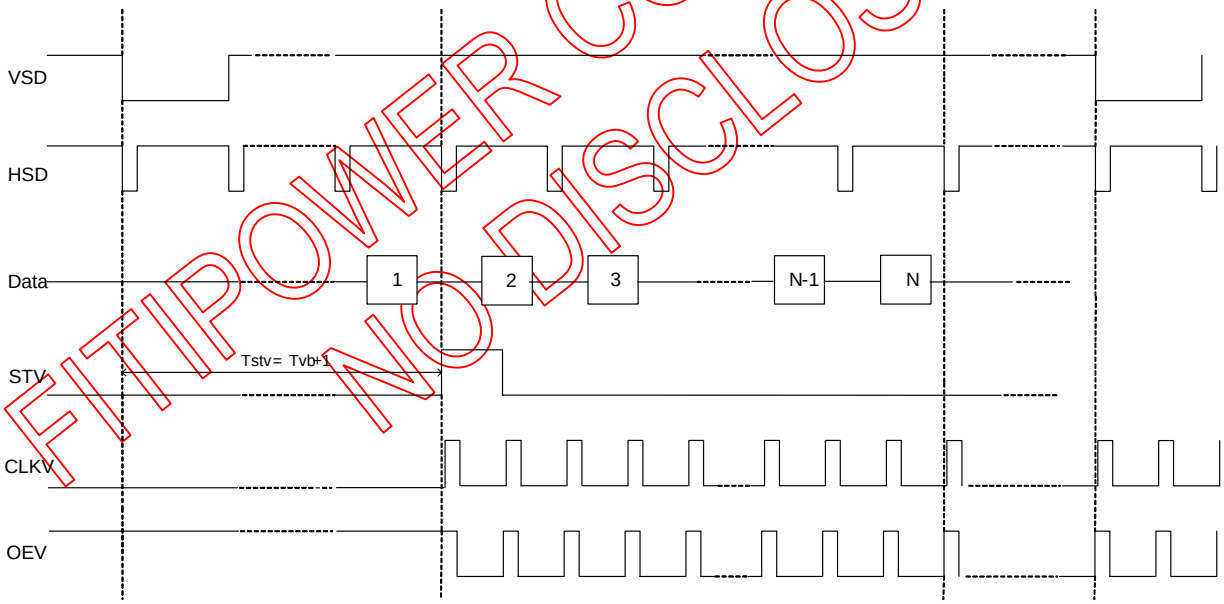
Vertical Timing Diagram HV (Cascade)



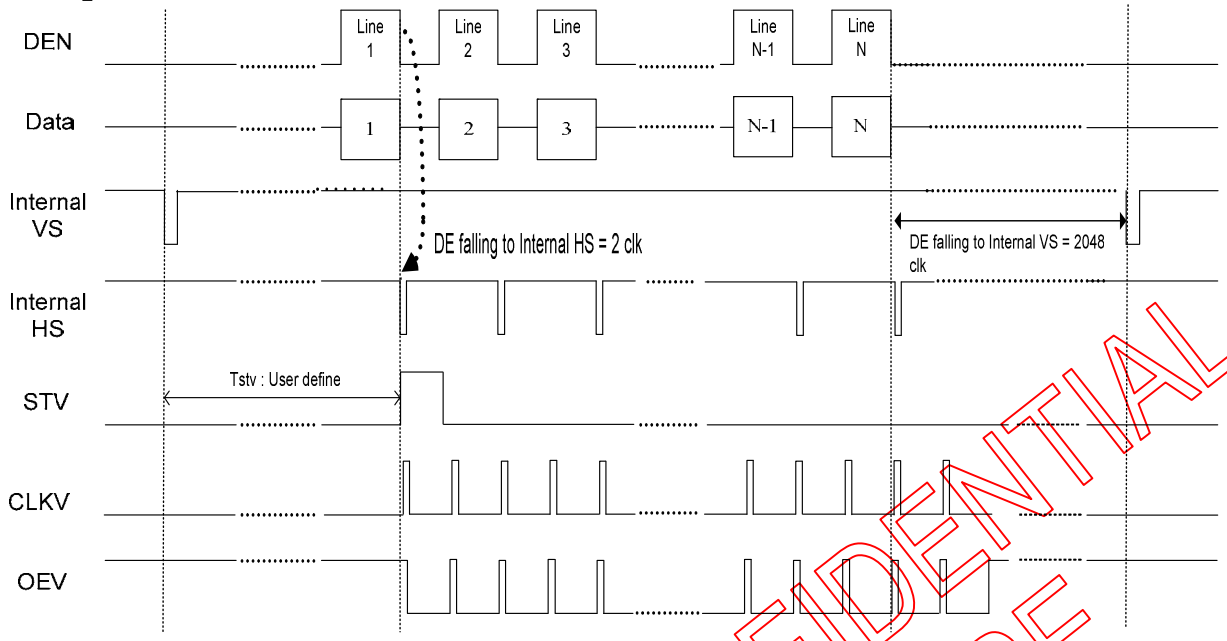
Vertical Timing Diagram DE (Cascade)



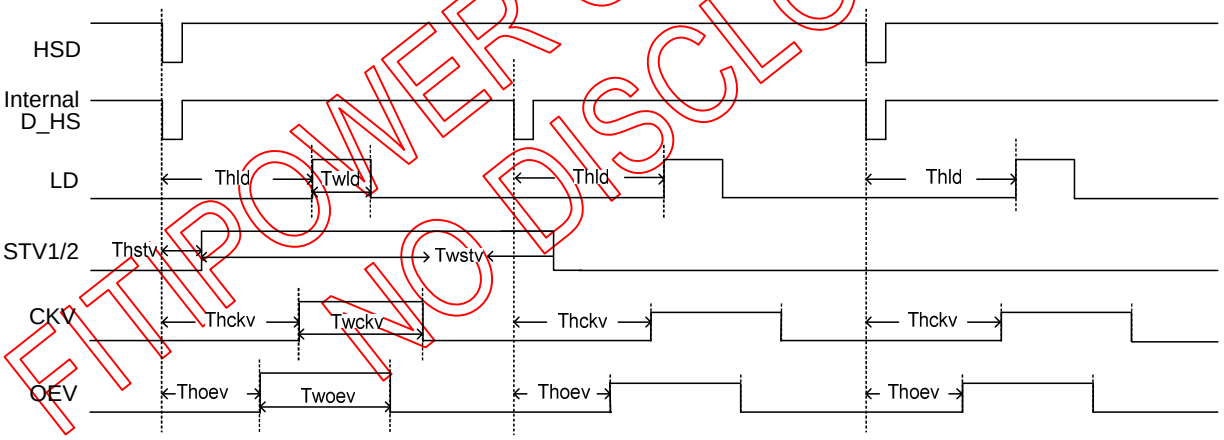
Gate Output Timing Diagram (Cascade)



Vertical Timing Diagram HV (Dual Gate)

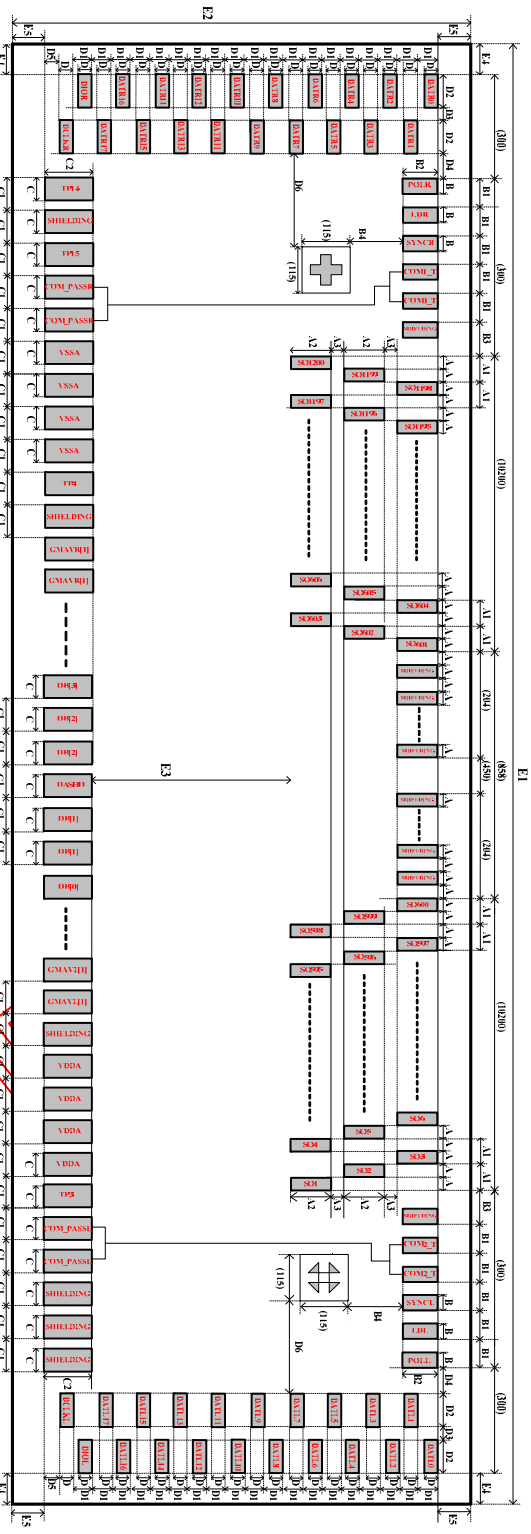


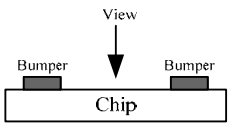
Vertical Timing Diagram DE (Dual Gate)



Gate Output Timing Diagram (Dual Gate)

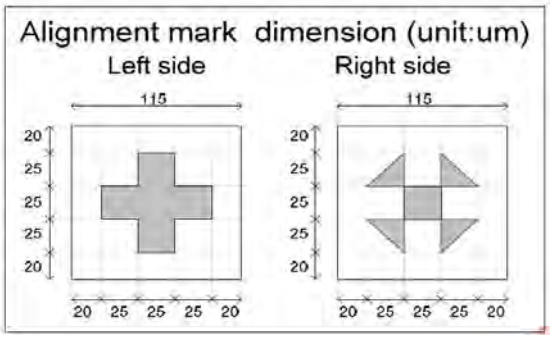
8. PAD OUTLINE DIMENSION





Pad Outline Dimension (Bump Side)

8.1. Alignment Mark



Alignment Mark

8.2. Pad Information

Symbol	Dimension(um)
A	17
A1	34
A2	110
A3	30
B	30
B1	50
B2	70
B3	50
B4	191.5
C	65
C1	85
C2	110

Symbol	Dimension(um)
D	30
D1	40
D2	100
D3	30
D4	70
D5	34
D6	168.5
E1	22572 (max) *
E2	938 (max) *
E3	324
E4	57 (max)
E5	57 (max)

*Note：Chip dimension includes scribe line

8.3. Pad Coordinates

No	Name	CX	CY
1	TP14	-10922.5	-357
2	SHIELDING[1]	-10837.5	-357
3	TP15	-10752.5	-357
4	COM_PASSR	-10667.5	-357
5	COM_PASSR	-10582.5	-357
6	VSSA	-10497.5	-357
7	VSSA	-10412.5	-357
8	VSSA	-10327.5	-357
9	VSSA	-10242.5	-357
10	TP4	-10157.5	-357
11	SHIELDING[2]	-10072.5	-357
12	GMAVR[1]	-9987.5	-357
13	GMAVR[1]	-9902.5	-357
14	SHIELDING[3]	-9817.5	-357
15	GMAVR[2]	-9732.5	-357
16	GMAVR[2]	-9647.5	-357
17	SHIELDING[4]	-9562.5	-357
18	GMAVR[3]	-9477.5	-357
19	GMAVR[3]	-9392.5	-357
20	SHIELDING[5]	-9307.5	-357
21	GMAVR[4]	-9222.5	-357
22	GMAVR[4]	-9137.5	-357
23	SHIELDING[6]	-9052.5	-357
24	GMAVR[5]	-8967.5	-357
25	GMAVR[5]	-8882.5	-357
26	SHIELDING[7]	-8797.5	-357
27	GMAVR[6]	-8712.5	-357
28	GMAVR[6]	-8627.5	-357
29	SHIELDING[8]	-8542.5	-357
30	GMAVR[7]	-8457.5	-357
31	GMAVR[7]	-8372.5	-357
32	SHIELDING[9]	-8287.5	-357
33	GMAVR[8]	-8202.5	-357
34	GMAVR[8]	-8117.5	-357
35	SHIELDING[10]	-8032.5	-357
36	GMAVR[9]	-7947.5	-357
37	GMAVR[9]	-7862.5	-357
38	SHIELDING[11]	-7777.5	-357
39	GMAVR[10]	-7692.5	-357
40	GMAVR[10]	-7607.5	-357
41	SHIELDING[12]	-7522.5	-357
42	GMAVR[11]	-7437.5	-357
43	GMAVR[11]	-7352.5	-357
44	SHIELDING[13]	-7267.5	-357
45	GMAVR[12]	-7182.5	-357
46	GMAVR[12]	-7097.5	-357
47	SHIELDING[14]	-7012.5	-357
48	GMAVR[13]	-6927.5	-357
49	GMAVR[13]	-6842.5	-357
50	SHIELDING[15]	-6757.5	-357
51	GMAVR[14]	-6672.5	-357
52	GMAVR[14]	-6587.5	-357
53	TP16	-6502.5	-357
54	TP0	-6417.5	-357
55	SHIELDING[16]	-6332.5	-357
56	SHIELDING[17]	-6247.5	-357
57	SHIELDING[18]	-6162.5	-357
58	SHIELDING[19]	-6077.5	-357
59	REV	-5992.5	-357
60	BIST	-5907.5	-357
61	BIST	-5822.5	-357
62	TP17	-5737.5	-357
63	VDDA	-5652.5	-357
64	VDDA	-5567.5	-357
65	VDDA	-5482.5	-357
66	VDDA	-5397.5	-357
67	SHIELDING[20]	-5312.5	-357
68	VSSA	-5227.5	-357
69	VSSA	-5142.5	-357
70	VSSA	-5057.5	-357
71	VSSA	-4972.5	-357
72	TP5	-4887.5	-357
73	VSS	-4802.5	-357
74	VSS	-4717.5	-357
75	VSS	-4632.5	-357
76	VSS	-4547.5	-357
77	TP6	-4462.5	-357
78	DIMO	-4377.5	-357
79	DIMO	-4292.5	-357
80	TP7	-4207.5	-357
81	VDD	-4122.5	-357
82	VDD	-4037.5	-357
83	VDD	-3952.5	-357
84	VDD	-3867.5	-357
85	TP1	-3782.5	-357
86	DBGATE	-3697.5	-357
87	DBGATE	-3612.5	-357
88	CSB	-3527.5	-357
89	MASL	-3442.5	-357
90	MASL	-3357.5	-357
91	SCL	-3272.5	-357
92	MASLOC	-3187.5	-357
93	MASLOC	-3102.5	-357
94	SDA	-3017.5	-357
95	RES[0]	-2932.5	-357
96	RES[0]	-2847.5	-357
97	CABC_EN[0]	-2762.5	-357
98	CABC_EN[1]	-2677.5	-357
99	RES[1]	-2592.5	-357
100	RES[1]	-2507.5	-357
101	CFSEL	-2422.5	-357
102	CFSEL	-2337.5	-357
103	DASHD[1]	-2252.5	-357
104	VSD	-2167.5	-357
105	VSD	-2082.5	-357
106	DASHD[2]	-1997.5	-357
107	HSD	-1912.5	-357

108	HSD	-1827.5	-357
109	DASHD[3]	-1742.5	-357
110	DEN	-1657.5	-357
111	DEN	-1572.5	-357
112	DASHD[4]	-1487.5	-357
113	CLKIN	-1402.5	-357
114	CLKIN	-1317.5	-357
115	DASHD[5]	-1232.5	-357
116	DB[7]	-1147.5	-357
117	DB[7]	-1062.5	-357
118	DB[6]	-977.5	-357
119	DB[6]	-892.5	-357
120	DASHD[6]	-807.5	-357
121	DB[5]	-722.5	-357
122	DB[5]	-637.5	-357
123	DB[4]	-552.5	-357
124	DB[4]	-467.5	-357
125	DASHD[7]	-382.5	-357
126	DB[3]	-297.5	-357
127	DB[3]	-212.5	-357
128	DB[2]	-127.5	-357
129	DB[2]	-42.5	-357
130	DASHD[8]	42.5	-357
131	DB[1]	127.5	-357
132	DB[1]	212.5	-357
133	DB[0]	297.5	-357
134	DB[0]	382.5	-357
135	DASHD[9]	467.5	-357
136	DG[7]	552.5	-357
137	DG[7]	637.5	-357
138	DG[6]	722.5	-357
139	DG[6]	807.5	-357
140	DASHD[10]	892.5	-357
141	DG[5]	977.5	-357
142	DG[5]	1062.5	-357
143	DG[4]	1147.5	-357
144	DG[4]	1232.5	-357
145	DASHD[11]	1317.5	-357
146	DG[3]	1402.5	-357
147	DG[3]	1487.5	-357
148	DG[2]	1572.5	-357
149	DG[2]	1657.5	-357
150	DASHD[12]	1742.5	-357
151	DG[1]	1827.5	-357
152	DG[1]	1912.5	-357
153	DG[0]	1997.5	-357
154	DG[0]	2082.5	-357
155	DASHD[13]	2167.5	-357
156	DR[7]	2252.5	-357
157	DR[7]	2337.5	-357
158	DR[6]	2422.5	-357
159	DR[6]	2507.5	-357
160	DASHD[14]	2592.5	-357
161	DR[5]	2677.5	-357
162	DR[5]	2762.5	-357
163	DR[4]	2847.5	-357
164	DR[4]	2932.5	-357
165	DASHD[15]	3017.5	-357
166	DR[3]	3102.5	-357
167	DR[3]	3187.5	-357
168	DR[2]	3272.5	-357
169	DR[2]	3357.5	-357
170	DASHD[16]	3442.5	-357
171	DR[1]	3527.5	-357
172	DR[1]	3612.5	-357
173	DR[0]	3697.5	-357
174	DR[0]	3782.5	-357
175	DASHD[17]	3867.5	-357
176	TP13	3952.5	-357
177	MODE	4037.5	-357
178	MODE	4122.5	-357
179	CLKPOL	4207.5	-357
180	CLKPOL	4292.5	-357
181	TP8	4377.5	-357
182	DITHB	4462.5	-357
183	DITHB	4547.5	-357
184	TP9	4632.5	-357
185	SHLR	4717.5	-357
186	SHLR	4802.5	-357
187	SHIELDING[21]	4887.5	-357
188	UPDN	4972.5	-357
189	UPDN	5057.5	-357
190	TP10	5142.5	-357
191	STBYB	5227.5	-357
192	STBYB	5312.5	-357
193	TP11	5397.5	-357
194	RSTB	5482.5	-357
195	RSTB	5567.5	-357
196	TP12	5652.5	-357
197	VDD	5737.5	-357
198	VDD	5822.5	-357
199	VDD	5907.5	-357
200	VDD	5992.5	-357
201	CAS	6077.5	-357
202	VSS	6162.5	-357
203	VSS	6247.5	-357
204	VSS	6332.5	-357
205	VSS	6417.5	-357
206	TP2	6502.5	-357
207	GMAVL[14]	6587.5	-357
208	GMAVL[14]	6672.5	-357
209	SHIELDING[22]	6757.5	-357
210	GMAVL[13]	6842.5	-357
211	GMAVL[13]	6927.5	-357
212	SHIELDING[23]	7012.5	-357
213	GMAVL[12]	7097.5	-357
214	GMAVL[12]	7182.5	-357
215	SHIELDING[24]	7267.5	-357
216	GMAVL[11]	7352.5	-357
217	GMAVL[11]	7437.5	-357
218	SHIELDING[25]	7522.5	-357
219	GMAVL[10]	7607.5	-357
220	GMAVL[10]	7692.5	-357
221	SHIELDING[26]	7777.5	-357
222	GMAVL[9]	7862.5	-357
223	GMAVL[9]	7947.5	-357
224	SHIELDING[27]	8032.5	-357

225	GMAVL[8]	8117.5	-357
226	GMAVL[8]	8202.5	-357
227	SHIELDING[28]	8287.5	-357
228	GMAVL[7]	8372.5	-357
229	GMAVL[7]	8457.5	-357
230	SHIELDING[29]	8542.5	-357
231	GMAVL[6]	8627.5	-357
232	GMAVL[6]	8712.5	-357
233	SHIELDING[30]	8797.5	-357
234	GMAVL[5]	8882.5	-357
235	GMAVL[5]	8967.5	-357
236	SHIELDING[31]	9052.5	-357
237	GMAVL[4]	9137.5	-357
238	GMAVL[4]	9222.5	-357
239	SHIELDING[32]	9307.5	-357
240	GMAVL[3]	9392.5	-357
241	GMAVL[3]	9477.5	-357
242	SHIELDING[33]	9562.5	-357
243	GMAVL[2]	9647.5	-357
244	GMAVL[2]	9732.5	-357
245	SHIELDING[34]	9817.5	-357
246	GMAVL[1]	9902.5	-357
247	GMAVL[1]	9987.5	-357
248	SHIELDING[35]	10072.5	-357
249	VDDA	10157.5	-357
250	VDDA	10242.5	-357
251	VDDA	10327.5	-357
252	VDDA	10412.5	-357
253	TP3	10497.5	-357
254	COM_PASSL	10582.5	-357
255	COM_PASSL	10667.5	-357
256	SHIELDING[36]	10752.5	-357
257	SHIELDING[37]	10837.5	-357
258	SHIELDING[38]	10922.5	-357
259	DCLKL	11049	-363
260	DIOL	11179	-323
261	DATL[17]	11049	-283
262	DATL[16]	11179	-243
263	DATL[15]	11049	-203
264	DATL[14]	11179	-163
265	DATL[13]	11049	-123
266	DATL[12]	11179	-83
267	DATL[11]	11049	-43
268	DATL[10]	11179	-3
269	DATL[9]	11049	37
270	DATL[8]	11179	77
271	DATL[7]	11049	117
272	DATL[6]	11179	157
273	DATL[5]	11049	197
274	DATL[4]	11179	237
275	DATL[3]	11049	277
276	DATL[2]	11179	317
277	DATL[1]	11049	357
278	DATL[0]	11179	397
279	POLL	10914	377
280	LDL	10864	377
281	SYNCL	10814	377
282	COM2_T	10764	377
283	COM2_T	10714	377
284	SHIELDING[39]	10664	377
285	SO[1]	10620.5	77
286	SO[2]	10603.5	217
287	SO[3]	10586.5	357
288	SO[4]	10569.5	77
289	SO[5]	10552.5	217
290	SO[6]	10535.5	357
291	SO[7]	10518.5	77
292	SO[8]	10501.5	217
293	SO[9]	10484.5	357
294	SO[10]	10467.5	77
295	SO[11]	10450.5	217
296	SO[12]	10433.5	357
297	SO[13]	10416.5	77
298	SO[14]	10399.5	217
299	SO[15]	10382.5	357
300	SO[16]	10365.5	77
301	SO[17]	10348.5	217
302	SO[18]	10331.5	357
303	SO[19]	10314.5	77
304	SO[20]	10297.5	217
305	SO[21]	10280.5	357
306	SO[22]	10263.5	77
307	SO[23]	10246.5	217
308	SO[24]	10229.5	357
309	SO[25]	10212.5	77
310	SO[26]	10195.5	217
311	SO[27]	10178.5	357
312	SO[28]	10161.5	77
313	SO[29]	10144.5	217
314	SO[30]	10127.5	357
315	SO[31]	10110.5	77
316	SO[32]	10093.5	217
317	SO[33]	10076.5	357
318	SO[34]	10059.5	77
319	SO[35]	10042.5	217
320	SO[36]	10025.5	357
321	SO[37]	10008.5	77
322	SO[38]	9991.5	217
323	SO[39]	9974.5	357
324	SO[40]	9957.5	77
325	SO[41]	9940.5	217
326	SO[42]	9923.5	357
327	SO[43]	9906.5	77
328	SO[44]	9889.5	217
329	SO[45]	9872.5	357
330	SO[46]	9855.5	77
331	SO[47]	9838.5	217
332	SO[48]	9821.5	357
333	SO[49]	9804.5	77
334	SO[50]	9787.5	217
335	SO[51]	9770.5	357
336	SO[52]	9753.5	77
337	SO[53]	9736.5	217
338	SO[54]	9719.5	357

339	SO[55]	9702.5	77
340	SO[56]	9685.5	217
341	SO[57]	9668.5	357
342	SO[58]	9651.5	77
343	SO[59]	9634.5	217
344	SO[60]	9617.5	357
345	SO[61]	9600.5	77
346	SO[62]	9583.5	217
347	SO[63]	9566.5	357
348	SO[64]	9549.5	77
349	SO[65]	9532.5	217
350	SO[66]	9515.5	357
351	SO[67]	9498.5	77
352	SO[68]	9481.5	217
353	SO[69]	9464.5	357
354	SO[70]	9447.5	77
355	SO[71]	9430.5	217
356	SO[72]	9413.5	357
357	SO[73]	9396.5	77
358	SO[74]	9379.5	217
359	SO[75]	9362.5	357
360	SO[76]	9345.5	77
361	SO[77]	9328.5	217
362	SO[78]	9311.5	357
363	SO[79]	9294.5	77
364	SO[80]	9277.5	217
365	SO[81]	9260.5	357
366	SO[82]	9243.5	77
367	SO[83]	9226.5	217
368	SO[84]	9209.5	357
369	SO[85]	9192.5	77
370	SO[86]	9175.5	217
371	SO[87]	9158.5	357
372	SO[88]	9141.5	77
373	SO[89]	9124.5	217
374	SO[90]	9107.5	357
375	SO[91]	9090.5	77
376	SO[92]	9073.5	217
377	SO[93]	9056.5	357
378	SO[94]	9039.5	77
379	SO[95]	9022.5	217
380	SO[96]	9005.5	357
381	SO[97]	8988.5	77
382	SO[98]	8971.5	217
383	SO[99]	8954.5	357
384	SO[100]	8937.5	77
385	SO[101]	8920.5	217
386	SO[102]	8903.5	357
387	SO[103]	8886.5	77
388	SO[104]	8869.5	217
389	SO[105]	8852.5	357
390	SO[106]	8835.5	77
391	SO[107]	8818.5	217
392	SO[108]	8801.5	357
393	SO[109]	8784.5	77
394	SO[110]	8767.5	217
395	SO[111]	8750.5	357
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888	SHIELDING[43]	301.5	357
889	SHIELDING[44]	267.5	357
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1405	SO[1109]	-9073.5	217
1406	SO[1110]	-9090.5	77
1407	SO[1111]	-9107.5	357
1408	SO[1112]	-9124.5	217
1409	SO[1113]	-9141.5	77
1410	SO[1114]	-9158.5	357
1411	SO[1115]	-9175.5	217
1412	SO[1116]	-9192.5	77
1413	SO[1117]	-9209.5	357
1414	SO[1118]	-9226.5	217
1415	SO[1119]	-9243.5	77
1416	SO[1120]	-9260.5	357
1417	SO[1121]	-9277.5	217
1418	SO[1122]	-9294.5	77
1419	SO[1123]	-9311.5	357
1420	SO[1124]	-9328.5	217
1421	SO[1125]	-9345.5	77
1422	SO[1126]	-9362.5	357
1423	SO[1127]	-9379.5	217
1424	SO[1128]	-9396.5	77
1425	SO[1129]	-9413.5	357
1426	SO[1130]	-9430.5	217
1427	SO[1131]	-9447.5	77
1428	SO[1132]	-9464.5	357
1429	SO[1133]	-9481.5	217
1430	SO[1134]	-9498.5	77
1431	SO[1135]	-9515.5	357
1432	SO[1136]	-9532.5	217
1433	SO[1137]	-9549.5	77
1434	SO[1138]	-9566.5	357
1435	SO[1139]	-9583.5	217
1436	SO[1140]	-9600.5	77
1437	SO[1141]	-9617.5	357
1438	SO[1142]	-9634.5	217
1439	SO[1143]	-9651.5	77
1440	SO[1144]	-9668.5	357
1441	SO[1145]	-9685.5	217
1442	SO[1146]	-9702.5	77
1443	SO[1147]	-9719.5	357
1444	SO[1148]	-9736.5	217
1445	SO[1149]	-9753.5	77
1446	SO[1150]	-9770.5	357
1447	SO[1151]	-9787.5	217
1448	SO[1152]	-9804.5	77
1449	SO[1153]	-9821.5	357
1450	SO[1154]	-9838.5	217
1451	SO[1155]	-9855.5	77
1452	SO[1156]	-9872.5	357
1453	SO[1157]	-9889.5	217
1454	SO[1158]	-9906.5	77
1455	SO[1159]	-9923.5	357
1456	SO[1160]	-9940.5	217
1457	SO[1161]	-9957.5	77
1458	SO[1162]	-9974.5	357
1459	SO[1163]	-9991.5	217
1460	SO[1164]	-10008.5	77
1461	SO[1165]	-10025.5	357
1462	SO[1166]	-10042.5	217
1463	SO[1167]	-10059.5	77
1464	SO[1168]	-10076.5	357
1465	SO[1169]	-10093.5	217
1466	SO[1170]	-10110.5	77
1467	SO[1171]	-10127.5	357
1468	SO[1172]	-10144.5	217
1469	SO[1173]	-10161.5	77
1470	SO[1174]	-10178.5	357
1471	SO[1175]	-10195.5	217
1472	SO[1176]	-10212.5	77
1473	SO[1177]	-10229.5	357
1474	SO[1178]	-10246.5	217
1475	SO[1179]	-10263.5	77
1476	SO[1180]	-10280.5	357
1477	SO[1181]	-10297.5	217
1478	SO[1182]	-10314.5	77

1479	SO[1183]	-10331.5	357
1480	SO[1184]	-10348.5	217
1481	SO[1185]	-10365.5	77
1482	SO[1186]	-10382.5	357
1483	SO[1187]	-10399.5	217
1484	SO[1188]	-10416.5	77
1485	SO[1189]	-10433.5	357
1486	SO[1190]	-10450.5	217
1487	SO[1191]	-10467.5	77
1488	SO[1192]	-10484.5	357
1489	SO[1193]	-10501.5	217
1490	SO[1194]	-10518.5	77
1491	SO[1195]	-10535.5	357
1492	SO[1196]	-10552.5	217
1493	SO[1197]	-10569.5	77
1494	SO[1198]	-10586.5	357
1495	SO[1199]	-10603.5	217
1496	SO[1200]	-10620.5	77
1497	SHIELDING[52]	-10664	377
1498	COM1_T	-10714	377
1499	COM1_T	-10764	377
1500	SYNCR	-10814	377
1501	LDR	-10864	377
1502	POLR	-10914	377
1503	DATR[0]	-11179	397
1504	DATR[1]	-11049	357
1505	DATR[2]	-11179	317
1506	DATR[3]	-11049	277
1507	DATR[4]	-11179	237
1508	DATR[5]	-11049	197
1509	DATR[6]	-11179	157
1510	DATR[7]	-11049	117
1511	DATR[8]	-11179	77
1512	DATR[9]	-11049	37
1513	DATR[10]	-11179	-3
1514	DATR[11]	-11049	-43
1515	DATR[12]	-11179	-83
1516	DATR[13]	-11049	-123
1517	DATR[14]	-11179	-163
1518	DATR[15]	-11049	-203
1519	DATR[16]	-11179	-243
1520	DATR[17]	-11049	-283
1521	DIOR	-11179	-323
1522	DCLKR	-11049	-363
-	ALIGN_L	-10773	93
-	ALIGN_R	10773	93

9. DEFINITIONS

9.1. Data Sheet Status

Preliminary Data Sheet	This data sheet contains preliminary data; supplementary data may be published later.
Data Sheet	This data sheet contains final product specifications.

Contents in the document are subject to change without notice.

9.2. Life Support Application

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. fitipower customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify fitipower for any damages resulting from such improper use or sale.

10. REVISION HISTORY

Revision	Content	Page	Date
0.1	New Issue.	--	2011/02/11
0.2	Modify HFRC function default value	17	2012/01/31
0.3	Modify gamma correction resistor	22.23.24	2012/05/21
0.4	Modify Time from HSD to Source Output Modify Time from HSD to LD	30	2012/07/31

APPENDIX A : BIST PATTERN

R→G→B→Black→White→Color Bar→Horizontal 256 gray scale→Vertical 256 gray scale→Crosstalk pattern→Chess board (L255/L0)→Flicker pattern→Black background with white out frame